# Hybrid Multi-Level Inverters Implemented in Photovoltaic Systems

# قلابات الفولتية الهجينية متعددة المستويات في انظمة الطاقة الكهروضوئية


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This Thesis was submitted in partial fulfillment of the requirements for the Master's Degree in Electrical Engineering from the Faculty of Engineering and Technology at Birzeit University, Palestine

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# Declaration of Authorship

I declare that this thesis entitled “Hybrid Multi-Level Inverters Implemented in Photovoltaic Systems” is the result of my own research except as cited in the references. It is being submitted to the Master’s Degree in Electrical Engineering from the Faculty of Engineering and Technology at Birzeit University, Palestine. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

Signed:

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Date:

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# Abstract

This thesis focuses on new Hybrid Multi-Level Inverters and their applications in the Photovoltaic systems. Both voltage and Current Source Inverters were surveyed, studied, some of them were simulated and analyzed using MATLAB/Simulink software. A comparison between the MLIs and HMLIs was conducted at the end of this thesis. Detailed analysis was done on the HMLI focusing on the Asymmetrical H-Bridge topology. It was studied under various environmental factors including irradiance and temperature. Also, the functionality of the control process of the inverter was investigated under variation of the load and different values of reference active power, reactive power and DC-link voltage. The results showed that, the inverter and the adaptive control process succeeded in producing a robust inverter that can be operated in different modes of power injection and had a high immunity against various weather conditions.

# المستخلص

تركز هذه الرسالة على القلابات الهجينة متعددة المستويات الجديدة وتطبيقاتها في الأنظمة الكهروضوئية. لقد تم مسح ودراسة ومحاكاة وتحليل كل من الجهد وقلاب الجهد المقترح باستخدام برنامجMATLAB\SIMULINK. وقد تم إجراء مقارنة ما بين القلابات الهجينة والقلابات متعددة المستويات في نهاية هذه الرسالة. وقد تم أيضا إجراء تحليل مفصل على HMLI مع التركيز على أساس H-Bridge غير متكافئة مداخل الجهد باعتماد التناظر الثلاثي. أيضا تمت دراسة القلاب الهجين في الرسالة تحت عوامل بيئية مختلفة بما في ذلك الإشعاع ودرجة الحرارة. بالإضافة إلى التحقيق في وظيفة عملية التحكم في القلاب تحت تغير الحمل والقيم المختلفة التي تشير إلى الطاقة الفعالة والقدرة التفاعلية و جهد المدخل الكامل. أوضحت النتائج أن القلاب وعملية التحكم المتكيفة قد نجحا في إنتاج قلاب قوي يمكن أن يعمل في أوضاع مختلفة لتزويد الطاقة للشبكة , وله مناعة عالية ضد الظروف الجوية المختلفة.

# Index Terms

Hybrid Multi-Level Inverter

PV Grid-Tied Inverters

Grid-Tied Inverters Control Process

LCL Coupling Filters

# Table of Contents

# Acronyms and Abbreviations

| | |
|---|---|
| **CSI** | Current Source Inverter |
| **FFT** | Fast Fourier Transform |
| **HMLI** | Hybrid Multi Level Inverter |
| **LS-SPWM** | Level-Shift Sinusoidal Pulse Width Modulation |
| **MLI** | Multi-Level Inverter |
| **MPPT** | Maximum Power Point Tracker |
| **P&O** | Perturb and Observer |
| **PS-SPWM** | Phase-Shift Sinusoidal Pulse Width Modulation |
| **PV** | Photovoltaic |
| **PWM** | Pulse Width Modulation |
| **RES** | Renewable Energy Sources |
| **SPWM** | Sinusoidal Pulse Width Modulation |
| **THD** | Total Harmonic Distortion |
| **THMLI** | Trinary Hybrid Multi Level Inverter |
| **VSI** | Voltage Source Inverter |

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# Chapter 1. Introduction

Despite the attractive features of renewable energy resources such as availability, sustainability, and being environment friendly, more challenges regarding their utilization and implementation in power systems have to be tackled.

## 1.1 Introduction

It has been very attractive for researchers to propose new technologies that facilitate human's life and solve their technical problems. Among their trend to increase the use of clean energy resources, the focus on developing power electronics devices is increasing enormously. This thesis focuses on studying one of the most important parts of the Photovoltaic (PV) system, which is the DC-to-AC converter; especially studying the latest updated topologies in the last two decades; "the Hybrid Multi-Level Inverters (HMLI)". Most HMLI used in the PV application will be selected, studied, simulated and analyzed. Specific indices will be chosen within this thesis, to determine the most appropriate and efficient topology that would be the best in PV applications.

## 1.2 Problem Statements

The Hybrid Multi-Level Inverter with both types of sources (voltage and current) are surveyed, studied and analyzed. This work implements hybrid inverters in photovoltaic systems applications. A comparison between voltage and Current Source Inverters is held to get the most efficient inverter that would be used in photovoltaic systems.

## 1.3 Contribution

This thesis proposes the implementation of the Trinary Hybrid Multi-Level Inverter in the PV systems. The contributions of the thesis can be described as follows:

- Introduction of a modular inverter with 3 different levels of voltages. That provides flexible design and easy maintenance procedures.
- Providing a design topology capable to accommodate the various conditions of environmental conditions.
- Providing a comprehensive and adaptive control method for the injected power into the grid and the DC-link voltage.

## 1.4 Research Goals

This research aims to:

- Present the latest Hybrid Multi-Level Inverters (HMLIs) recently proposed by researchers
- Hold a comparison between HMLIs based on many indexes mentioned later in this thesis
- Modeling the HMLI in a photovoltaic system, modeling, simulating and analyzing the results using MATLAB/Simulink

## 1.5 Organization of the Thesis

This thesis report is divided into eight chapters that have the following brief descriptions:

- Chapter 2 introduces the relationship between renewable energy sources and power electronic devices and demonstrates a brief historical introduction of power electronic converters and presents most problems that new technologies had solved in the last few decades. Also, it presents an introduction to the PV structure and popular algorithms and power electronic devices that are usually used within PV system implementation.
- Chapter 4 describes how and why researchers are in favor of replacing Multi-Level Inverters by the Hybrid Multi-Level Inverters. It demonstrates the most well-known voltage and current source Multi-Level Inverters. Besides, it presents most of the modulation techniques used to control Multi-Level Inverters. On the other side, it demonstrates the Hybrid Multi-Level Inverters surveyed through the literature review, lists their advantages and drawbacks, and compares between them using comparing indexes list within the thesis.
- Chapter 5 introduces the grid-tied inverters. It discusses the new technologies and topologies of them. It also focuses on the coupling filters between the inverters and the grid.
- Chapter 6 presents the design procedure for the whole parts of the inverter; starting from the PV system, boost converter, modulation techniques, coupling filter and controllers.
- Chapter 7 demonstrates the MATLAB model simulation and results. It discusses the results based on the theory described in the literature review.
- Chapter 8 draws out conclusions and sets out future work plan.

# Chapter 2. Literature Review

## 2.1 Introduction

The fast development of the Renewable Energy Systems (RESs) in the last few decades, made it very necessary to improve required power devices to make use of, especially the power converters and inverters. Continuous researches and studies were focused on various types of power electronic devices that convert power from AC to DC and vice versa. Starting from the most traditional one, the two-level converters, to the Multi-Level ones in the last two decades, and ending by the newest ones, the hybrid Multi-Level ones.

Although, they are very simple, traditional power inverters, which are also referred as two-level power inverters have many drawbacks. Their output harmonic components are very large, and so the Total Harmonic Distortion (THD) is very high. Since they are two-level inverter, the voltage variation with respect to time $\frac{dv}{dt}$ is very large, that makes sever stress on power switches of the inverter. Also, they operate on very high values of the switching frequency, which increases switching losses within the power electronic devices. On the other side, their application are limited to the low and medium voltage ranges [1], [2].

Multi-Level Inverters (MLIs) were first introduced in 1975 by Baker and Banisster [3]. They introduced the cascaded H-Bridge inverter. Then the Neutral Point Clamped inverter (NPC) was introduced by Baker in 1980 [4]. After that, the Flying Capacitor (FC) inverter was introduced by Meynard and Foch in 1992 as a modification to the NPC one, they used clamping capacitors instead of the diodes [5].

## 2.2 Features of Multi-Level Inverters

Multi-Level Inverters (MLIs) have many attractive features that raised their use in the last decades, which can be summarized as follows [1], [2], [6]–[8]:

**1- Staircase waveform quality**

Which means less $\frac{dv}{dt}$ rate, less stress across inverter switches and the Electromagnetic Compatibility (EMC) will be reduced accordingly. In addition, the harmonic components will be reduced in the output waveforms.

**2- Common-Mode Voltage (CM)**

A MLI produces smaller CM voltage. In motor drive application, the stress on the motor bearings will be reduced [1].

**3- Low distortion in the Input Current**

MLIs can draw input current with a low distortion [1].

**4- Wide Range of Switching Frequency**

On the contrary to the two-level inverters, the MLI can operate at both fundamental switching frequency and high switching frequency Pulse Width Modulation (PWM) schemes. That means less switching losses. And so, a more efficient inverter.

**5- Reduced Number of Components**

In some cases, newly proposed MLIs in recent researches have less components of power switches, diodes, or capacitors.

**6- Modular Topology (Redundancy)**

Some types of MLIs have the property of modularity. That means the ease of maintenance and more availability of output power.

Nevertheless, MLIs have some drawback that can be summarized as follows [2], [9]:

**1- High Number of Power Switches**

In most cases, the high number of the switches is the most important problem in the MLI.

**2- Control Complexity**

MLI must be precisely controlled to get the best required output waveform.

**3- Voltage balancing of the inverter capacitors**

Some types of MLIs face the problem of the unbalance voltages cross their capacitors. That is due certain operating conditions, the value of the modulation index, the dynamic behavior and load conditions [10].

## 2.3 What is Hybrid?

Due to the previous mentioned drawbacks of the conventional Multi-Level Inverters, researcher have been doing their best to introduce more kinds of inverters tackling those obstacles. Hybrid Multi-Level Inverters (HMLI) were introduced. Basically, HMLIs are derived as a combination of the conventional MLIs. That is what the word "Hybrid" points to. Actually, Hybrid corresponds to one of the followings [11]:

*1- Hybrid source:*

In this topology of inverters, the input power sources ,voltage or current, are different or unequal for each cell [7], [12], [13].

*2- Hybrid configuration:*

This topology of inverters has two or more type of conventional two-level inverters or Multi-Level ones [14].

*3- Hybrid device:*

In this topology, additional devices and power elements are added to the conventional topology of the MLI. This may include power diodes, capacitors, switches or transformers [15]–[17].

All possible Hybrid Multi-Level Inverters (HMLIs) are considered to solve one or more of the problems that the conventional Multi-Level Inverters face. They might reduce the harmonic components in the output waveform, and thus the value of Total Harmonic Distortion (THD). Also, they reduce the power switching and conduction losses in the reduced topologies of HMLI. HMLIs may be used to regulate the voltage among the DC link capacitors of the inverter, or to get more flexible number of output waveform levels.

Despite the huge number of the Multi-Level and Hybrid Multi-Level studies, focused on the voltage-source MLIs, very few studies focus on the current-source MLIs; the Multi-Level Current Source Inverter has drawn little concern. One can easily figure that, there are great

efforts and trials to classify voltage-source MLIs, but it’s the opposite for the current-source MLIs; whose classifications still need more and more attention and reviews [1], [7], [18].

## 2.4 Photovoltaic Systems

### 2.4.1 Introduction

The large technological and industrial revolution in the last couple of centuries depended mainly on the bulk demand of the fossil fuel. In the last few years, scientists declared that it would be difficult to depend completely on that type of fuel. That is because, it is a non-renewable source of energy, which has a relatively high cost, and has bad effects on environment and causes pollution.

Renewable energy resources began to take its role significantly in the last few decades. Photovoltaic (PV) solar system was one of the most importantly introduced resources. PV systems are clean, emission-free, and plentiful. Simply, the PV system converts the photon energy into electrical one. It basically consists of PV arrays, a DC-to-DC converter implementing a maximum power point tracker algorithm, and a DC-to-AC converter (inverter). The PV array consists of a multiple number of PV modules, each module consists of multiple solar cells, that can be electrically modelled as in Fig. 2-1 [19].

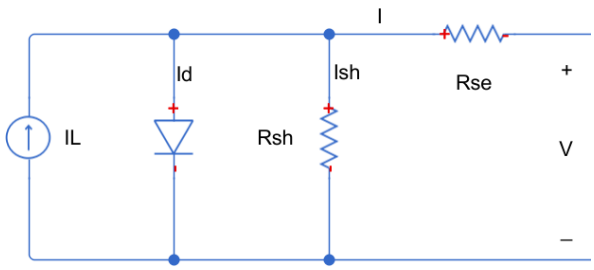


*Fig. 2-2-1 A PV cell equivalent circuit*

Actually, the output voltage and current of the solar cell depends on many factors. Thus, they always change as these factors change. Manufacturing materials, ambient temperature and the rate of radiation are the most effective factors that specify the output of the PV module. In addition, the current delivered to load also affects the PV module efficiency [13], [20]. It is desired to keep the power delivered out of the PV module as maximum as possible. Many algorithms were proposed to operate the PV module at a point that gives the maximum output power whatever the affecting factors were. These algorithms are called the Maximum Power Point Trackers (MPPT). One of the most common MPPT methods is the Perturb and Observe (P&O) [19]. Fig. 2-2 shows how to determine the Maximum Power Point (MPP) of a PV cell depending on the output power yield.

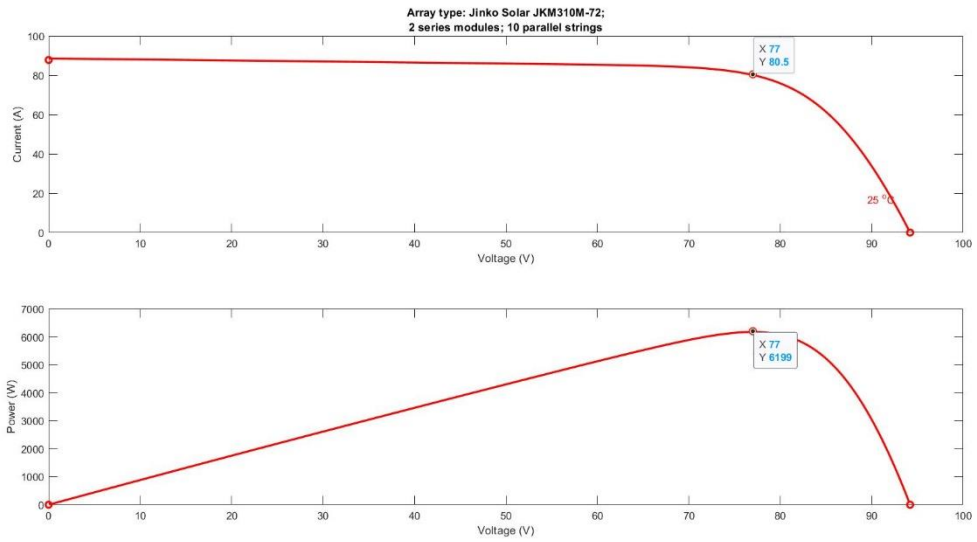


*Fig. 2-2-2 Maximum power point of a PV cell*

## 2.4.2 Perturb and Observer MPPT

One of the most popular MPPT algorithms is the Perturb and Observer (P&O) [19]. That is because it's simple and easy to implement. It basically depends on two mechanisms: 1) Perturb the input and 2) observe the output. The tracker tries to find the Maximum Power Point (MPP) by incrementing or decrementing the PV operating voltage and observing the resulting output power. The way of changing the PV voltage (incrementing or decrementing) in which the output power approaches to the value of the MPP must be kept and followed. But, if the output power value drifts away from the value of the MPP, the change in the voltage must be reversed. Fig. 2-3 depicts a flowchart explaining the method of the P&O algorithm.

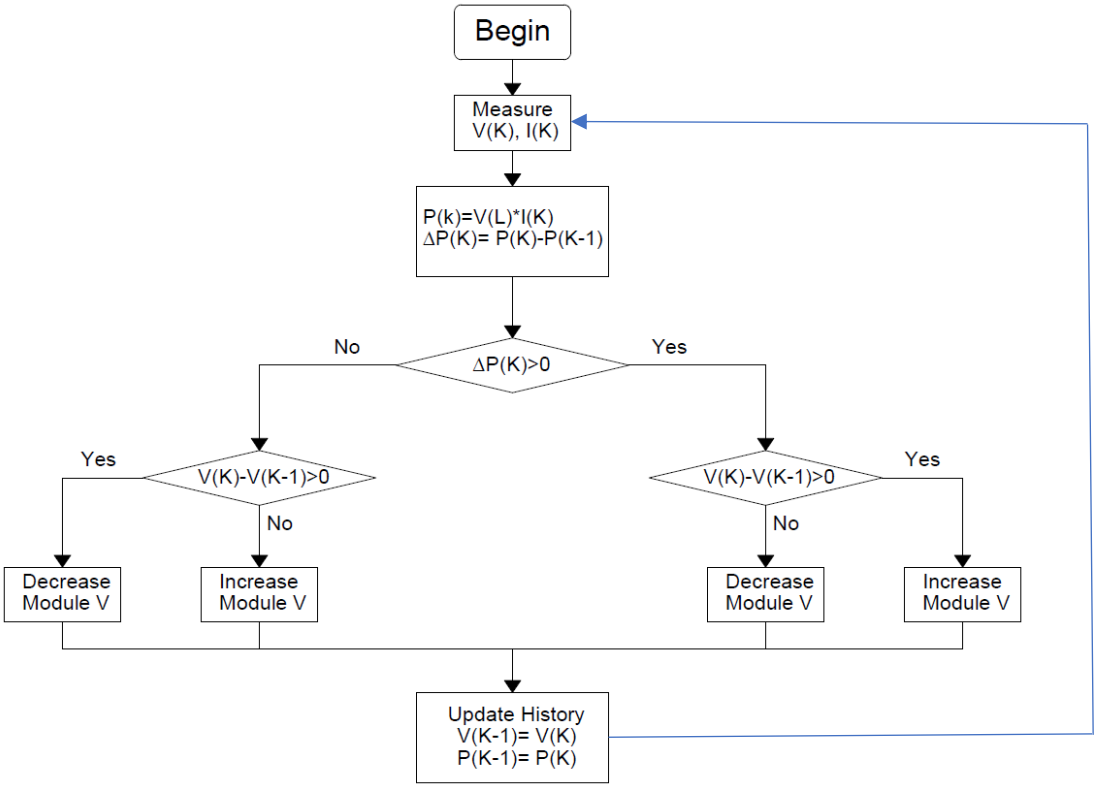


*Fig. 2-3 Perturb and Observer algorithm [19]*

In addition to achieving the maximum output power of the PV system, it is also required to get a stable DC output of the system that can act as a perfect input for the DC to AC converters. That could be achieved using a DC-to-DC converter. Depending on the desired output of the converter, the type (Boost, SEPIC or Cuk) and the input of the DC-to-DC converter can be easily determined.

### 2.4.3 Step-up (Boost) Converter

DC-to-DC converters are usually used in DC power supplies, Uninterruptable Power Supplies (UPSs), DC motor drives and renewable energy applications. The input of the DC-to-DC converter is usually unregulated DC voltage, which can be an output from a rectifier or an output for a Photovoltaic (PV) array system. It is common in these cases, to have an unstable output voltage that may have considerable variations and fluctuations.

It is used to use the Step-up (Boost) converters in the PhotoVoltaic (PV), to raise the output voltage of the PV array to a considerable value suitable for most applications [21]. As shown in Fig. 2-4, the Boost converter basically consists of a DC input voltage source $V_s$, Boost inductor L, controlled switch S, diode D, and a filter capacitor C.

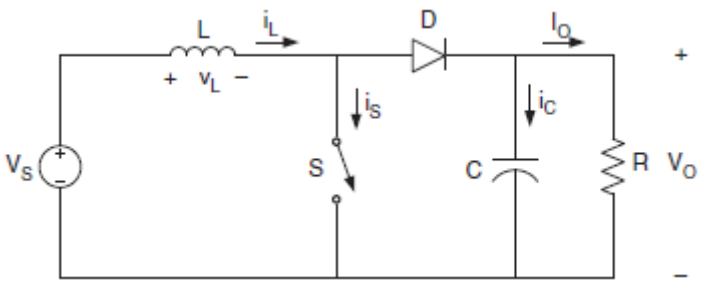


*Fig. 2-4 A Boost converter topology*

When the switch S is on, the current in the inductor increases linearly. And when it is off the current decrease linearly and the stored energy is dissipated in the RC circuit. Eq. (2.1) shows the relation between the input voltage $V_s$ and the output voltage $V_o$.

$$V_s DT = (V_o - V_s)(1 - D)T \tag{2.1}$$

where D is the duty ratio and is defined as the ratio between the switch on time to the sum of the on and off times. Accordingly, the relation between the output voltage and input voltage is described by eq. (2.2);

$$\frac{V_o}{V_s} = \frac{1}{1 - D} \tag{2.2}$$

# Chapter 3. Multi-Level and Hybrid Multi-Level Inverters

Mainly, Multi-Level and Hybrid Multi-Level Inverters are classified into two types; voltage-source inverters and current source inverters. It is common that, only different types of sources and loads can be connected to each other; the voltage source can be directly connected to a current type load and current sources can be directly connected to a voltage type load. The purpose of such criterion is to avoid the parallel connection between two voltage-type elements, and so preventing short-circuit between them or avoid connecting two current sources in series [22], [23].

## 3.1Voltage Source Inverters (VSIs)

The output waveform of this type of inverters is an independently controlled voltage waveform. It's a fully controlled magnitude, frequency and phase shift output. VSIs are very commonly used inverters as they naturally behave as voltage sources, that are required by most of industrial, medium and high voltage applications [1], [24].

VSIs are categorized into three main categories; the two-level inverters, Multi-Level Inverters and the Hybrid Multi-Level Inverters. Two-level inverters will not be taken into consideration here, the Multi-Level Inverters will be briefly described to get the concept of the Multi-Level techniques, and the Hybrid Multi-Level Inverters will be deeply described, analyzed and simulated.

### 3.1.1 Multi-Level Voltage Source Inverters

The shape of the output waveform for this type of inverters looks like a staircase. The number of levels varies from 3 up to 81 levels, or more. It depends on the inverter topology, number of switches and the modulation technique used. There are three basic types of Multi-Level Inverters commonly named traditional or conventional Multi-Level Inverters. Those are Neutral Point Clamped inverter, cascaded H-bridge inverter and Flying Capacitor inverter. Each of these inverter types can be configured or constructed depending on the number of used

switches and supporting diodes or capacitors to produce a different level type of the same schematic.

#### 3.1.1.1 Neutral Point Clamped (NPC) Inverter

It is also known as Diode Clamped inverter. It is one of the most common topologies for medium and high-level voltage applications, especially for motor drive applications. It has many advantages such as; reduced $dv/dt$ rate, reduced Total Harmonic Distortion (THD) and its ability to deal with high voltage demand without connecting switches in series [1], [22], [23]. However, it can be also used in low voltage applications such as the photovoltaic systems, where other factors like the voltage with low distortion and reduced leakage current are very important. Fig. 3-1 shows the three-phase three-level configuration of the NPC inverter. Whilst, Fig. 3-2 shows the output waveforms of the inverter, which shows the expected staircase shape of the output.

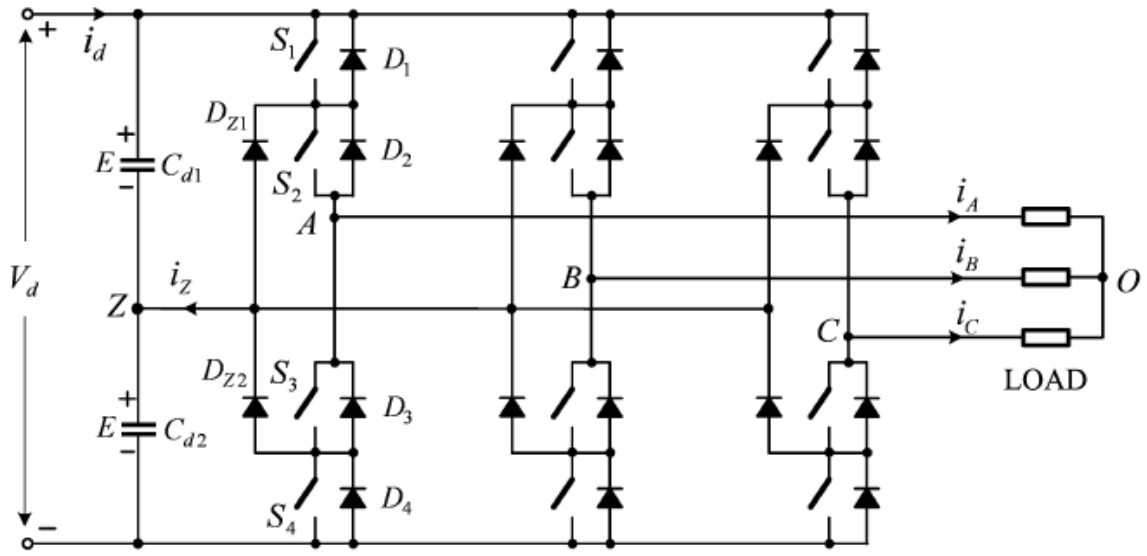


*Fig. 3-3-1 Three level three phase NPC inverter* [23]

NPC inverter has one major problem, which is related to the DC-link capacitor voltage and its control process. The neutral point voltage, $v_z$, varies with the operating conditions of the NPC inverter [22]. The DC-link capacitors are charged and discharged by the neutral current $i_z$, causing neutral-point voltage deviation. Besides, other factors may affect the neutral point voltages, such as [23]:

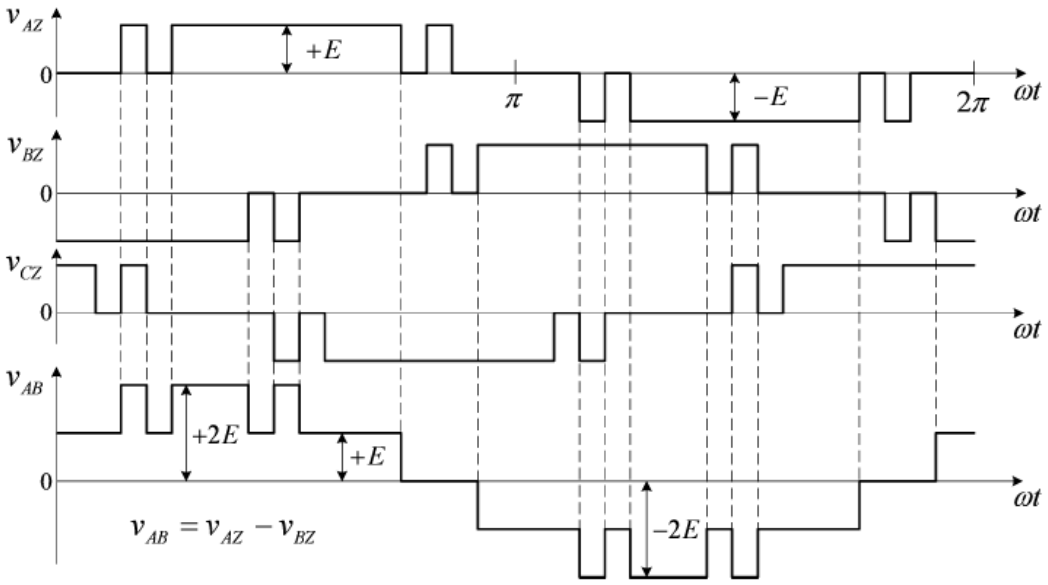


*Fig. 3-2 Line to line voltage waveform of the 3-level 3-ph NPC inverter* [23]

- Unbalanced DC capacitors due to manufacturing tolerances
- Inconsistency in switching device characteristics
- Unbalanced three-phase operations

Many control processes were introduced to solve the neutral point voltage deviation in the NPC inverter, where the voltage deviation is detected and then controlled again [25], [26]. In addition, although each active switching device is only required to block a voltage level of $V_{dc/(m-1)}$, the clamping diodes must have different voltage ratings for reverse voltage blocking [6]. Besides, as the number of required levels is increased, the control process of the NCP inverter becomes more complex.

#### 3.1.1.2 Cascaded H-Bridge Inverter

Cascaded H-bridge inverter is one of the most popular inverters used in medium voltage applications. It is constructed from multiple units of single-phase H-bridge power cell as shown in Fig. 3-3.

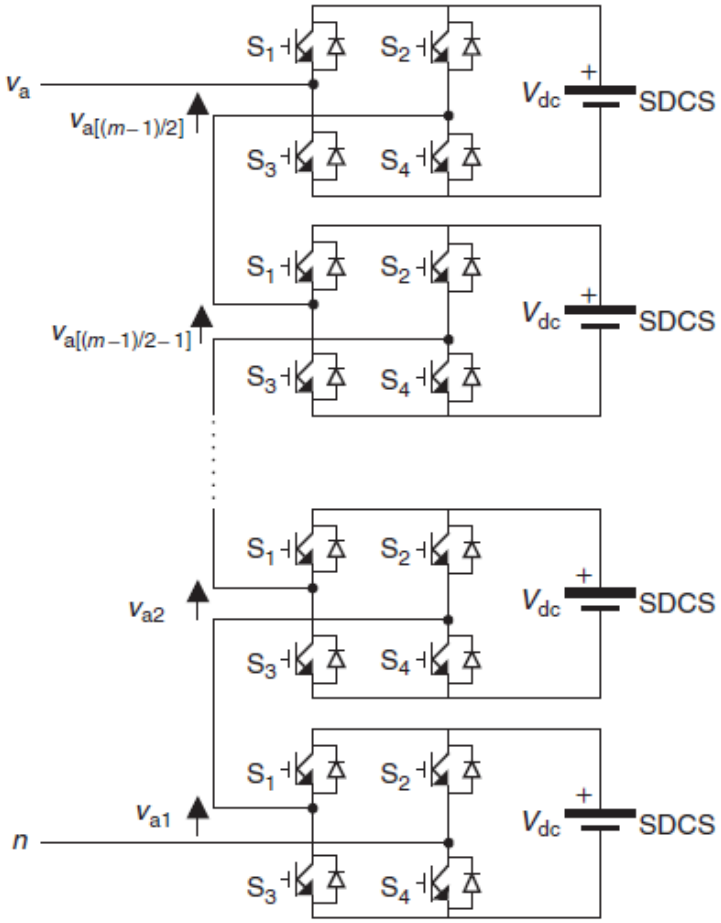


*Fig. 3-3 Single-phase H-bridge inverter*

Those single-phase H-bridge power cells are connected in cascade to get the desired medium voltage level and the low value of the total harmonic distortion. Practically, the number of cells is determined according to the operating voltage and the manufacturing cost. Actually, using equal DC H-bridge cells in the inverter leads to the property of modularity and therefore, a reduction of the manufacturing cost [23]. However, more levels can be obtained when unequal DC power supplies are used.

For equal DC sources, the level's number of the output waveform depends directly on the number of the used H-bridge cells of the inverter. It can be given by eq. (3.1).

$$m = 2H + 1 \tag{3.1}$$

Where, m is the number of the output levels, and H is the number of the single-phase H-bridge power cells. This equation is only valid for cascaded H-bridge inverters with equal DC voltage input of the cells (traditional H-bridge inverter). Inverters having different values for their input

cells have a different consideration according to the criterion followed in choosing the input DC voltages, and they will be discussed later in Chapter 4.

Cascaded H-bridge inverters have many advantages that other Multi-Level Inverters don't have, such as: (i) simple packaging and physical structure (ii) ability to operate during fault occurrence in one or more of H-bridge power cells (iii) modular structure which leads to fast and simple maintenance operations. However, they give some disadvantages such as: (i) high number of isolated DC sources (ii) complex control for increased number of output waveform levels. In PV system application, it is too easy to maintain the required DC voltage inputs for the cascaded H-bridge Multi-Level Inverter. That is the reason for the widespread use of them in such applications, and it will be also discussed later on in upcoming sections. Fig. 3-4 and Fig. 3-5 show different topologies of the cascaded H-bridge inverter that give 5, 7 and 9 levels, respectively.

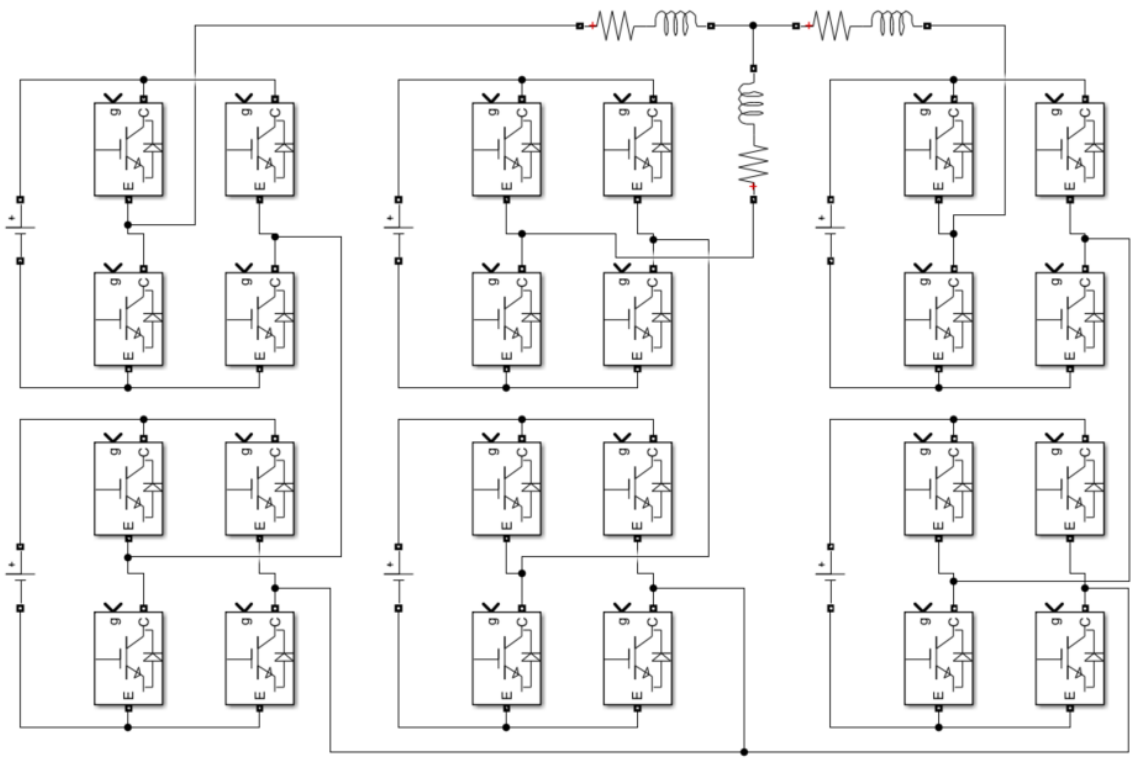

*Fig. 3-4 Five-level cascaded H-bridge inverter*

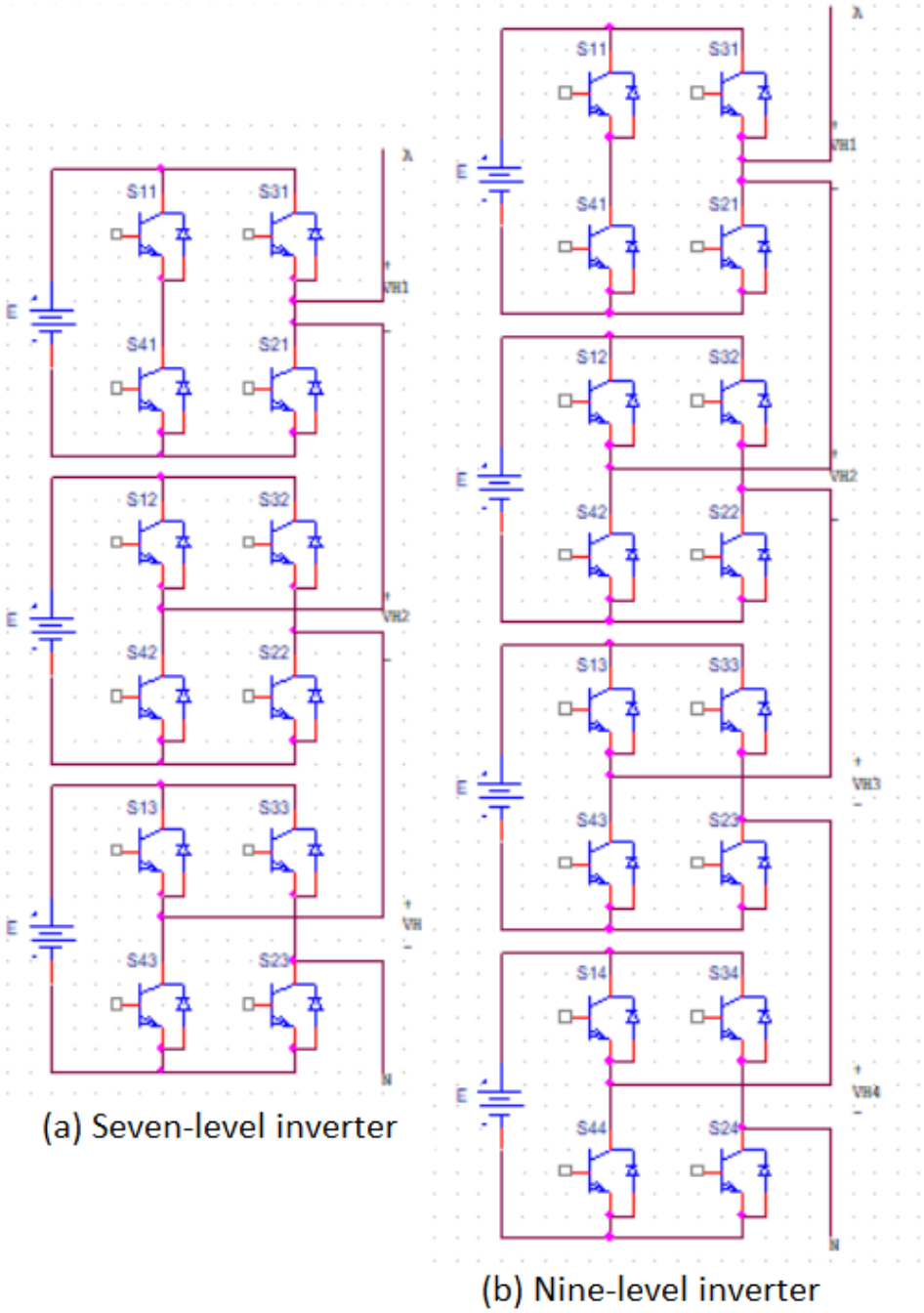


*Fig. 3-5 Per-phase topology of (a) seven- and (b) nine-level CHB inverters*

The total number of used switches in the cascaded H-bridge inverter is given by eq. (3.2)

$$N_{sw} = 2 * (\mathrm{m} - 1) \tag{3.2}$$

Where, m is also the number of desired levels in the output waveform.

### 3.1.1.3 Flying Capacitor Multi-Level Inverter

The structure of this inverter is similar to that of the diode-clamped inverter except that, instead of using clamping diodes, the inverter uses capacitors. On the contrary to the NPC inverters, Flying Capacitor inverters (FC) present higher degree of freedom (redundant states) to synthesize a specific output voltage and employ a lesser number of power electronic devices. This property of higher states of redundancy enables the inverter to regulate its capacitors' voltage correctly and easily [1], [2], [7], and [18]. In addition, the use of high frequency switching is recommended in the FC inverters to quickly balance the charge between the flying capacitors of the inverter. Fig. 3-6 shows different topologies of the FC inverters for different number of levels.

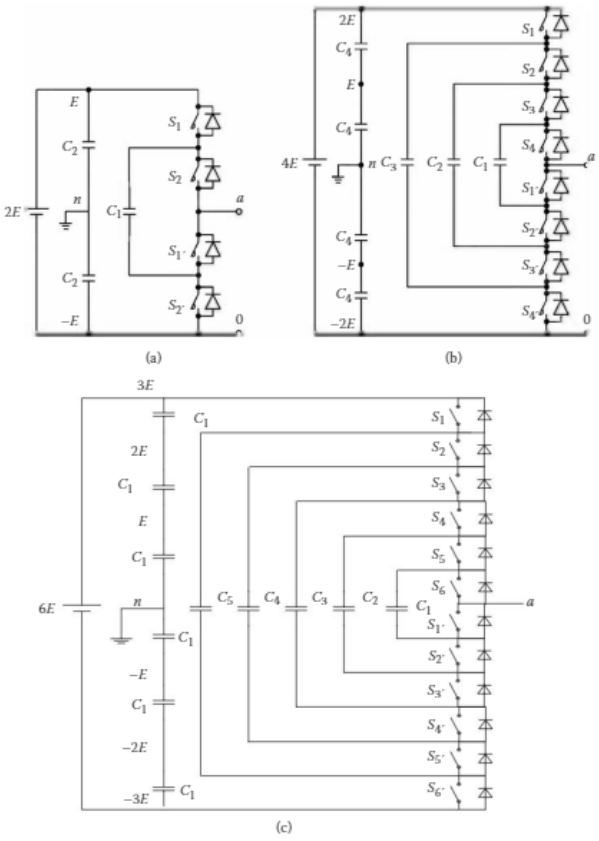


*Fig. 3-6 FC Multi-Level Inverter topologies for a) three levels, b) five levels and, c) seven levels* [7]

FC inverter has a modular structure and it is used widely in high frequency applications like the medium voltage traction systems. In addition, in the FC inverter both real and reactive power flow can be controlled and the large number of capacitors enable the inverter to ride through power outages and deep voltage sags. Similar to NPC inverters, for high number of levels topologies, the control process will be complicated, the switching utilization and inverter

efficiency are poor in real power transmission applications, the inverter cost will be very expensive and its size will be bulky [1], [2], and [23].

### 3.1.2 Hybrid Multi-Level Voltage Source Inverter

Nowadays, researchers focus their studies on proposing new hybrid inverters to overcome problems of the Multi-Level inverters related to the relative high number of the switches in some topologies, control complexity for high level inverters, DC isolated power supplies and the capacitor voltage regulations. Mainly, those Hybrid Multi-Level inverters are derived from the classical topologies of the Multi-Level Inverters mentioned previously. That is to meet the high grid code standards and the power quality issues in an economical way. There are many new topologies that are presented in literature, each has its own structure, applications, advantages and drawbacks. A review of various topologies will be listed, studied and analyzed. However, just a few of them will be considered and simulated using MATLAB/Simulink.

Hybrid Multi-Level inverters that will be presented and discussed are:

1- Mixed-Level Hybrid Multi-Level Inverters
2- Asymmetric Binary Hybrid Multi-Level Inverters (BHMLI)
3- Asymmetric Trinary Hybrid Multi-Level Inverters (THMLI)
4- Hybrid Multi-Level Inverter Using Switched Capacitor Units
5- Multi-Level DC-Link Inverter
6- Hybrid Multicell Converter Topology and Modulation
7- Hybrid Multi-Level Converter with Distinct Series Connected Cells [8][11].
8- Hybrid Asymmetric Multi-Level Inverter for Competitive Medium-Voltage Industrial Drives [28].
9- New Hybrid Asymmetrical H-bridge Multi-Level Inverter[29].
10- Hybrid Multi-Level Inverter with Single DC Source [30].

However, there are many other topologies such as:

1- New Symmetrical Hybrid Multi-Level DC-AC Converters
2- Hybrid-Clamped Multi-Level-Inverter Topologies
3- Hybrid Multi-Level Inverter based on main inverter and conditioning inverter [11][31].

Kala and Arora, in [2], divided the Hybrid Multi-Level Inverter into three main categories:

1- Reduced Components Count (RCC) topologies with H-bridge:

These types of Hybrid Multi-Level Inverters are mainly used in the Low Voltage (LV) and PV applications. They also have the separate polarity generation and level generation blocks. This category includes:

a- Developed Cascaded Multi-Level Inverter (DCMLI)
b- Cascaded Sub-Multi-Level Inverter (CSMLI)
c- Multi-Level DC Link Inverter (MLDCLI)
d- Hybrid Multi-Cell Converter (HMC)
e- Series Diode Clamped H-bridge Multi-Level Inverter (SDCHB MLI)
f- Switched Series/Parallel Sources Multi-Level Inverter (SSPS MLI)

2- Reduced Components Count (RCC) topologies without H-bridge:

This type of Hybrid Multi-Level Inverters is mainly considered for medium voltage (MV) applications. They consist of series connected unit cells with bipolar waveform generation capability. This category includes:

a- Cascaded Basic Blocks Multi-Level Inverter (CB MLI)
b- Cascaded Modified H-bridge Multi-Level Inverter (CMB MLI)
c- Chain Cell Multi-Level Inverter (CC MLI)
d- Cross Connected Sources Based Multi-Level Inverter (CCS MLI)
e- Level Doubling Network Based Cascaded MLI (LDNC MLI)
f- Switched Capacitor Cell Hybrid Multi-Level Inverter (SCH MLI)

3- Miscellaneous Hybrid Multi-Level Inverters

Some are mainly intended for medium and high voltage applications. Others utilize variable ratio transformers for producing a greater number of voltage levels while boosting the LV supply obtained from standalone PV arrays and fuel cells. These include:

a- Switched Ladder Multi-Level Inverter (SL MLI)
b- Asymmetrical Transistor Clamped H-bridge MLI (ATCHB MLI)
c- Nested Neutral Point Clamped (NNPC) Converter
d- Active Neutral Point Clamped (ANPC) Converter
e- Pulse Width Modulation Based Multi-Level Inverter (PWM MLI)

## 3.2 Current Source Inverters

The main objective of using Current Source Inverters (CSIs) is to generate an AC output waveform from a current DC source. The output current has a controllable magnitude, frequency and phase shift. It is common to use a capacitive filter with inductive load application. Since the DC bus is a current source type, it cannot be opened; therefore, at least there must be one switch closed at each moment of time. Thus, overlap periods are required. Although Current Source Inverters are less popular than the voltage source inverters, they have more advantages. They are widely used in High Voltage motor drive applications, and they are highly recommended in application were boosting capabilities are required [32]–[34].

Current Source Inverters are classified into the following types:

1- Pulse Width Modulated Current Source Inverters (PWM CSIs)
2- Parallel Current Source Inverters (PCSIs)
3- Load-Commutated Current Source Inverters (LC CSIs)
4- Boost Type Current Source Inverters (BT CSIs)
5- LC Current Source Inverters (CSIs)
6- Multi-Level Current Source Inverters (ML CSIs)
7- Hybrid Multi-Level Current Source Inverters (HML CSIs)

### 3.2.1 PWM Current Source Inverter

It consists of six switches divided as couples into three legs, the reason for naming it in some references as a three-phase full bridge Current Source Inverter. In some cases of MV/HV applications each switch can be replaced by two or more switches in order to raise the inverter's power capabilities [23]. All switches in the PWM CSI are identical and have a reverse voltage blocking capability. Fig. 3-7 shows the topology of the PWM CSI.

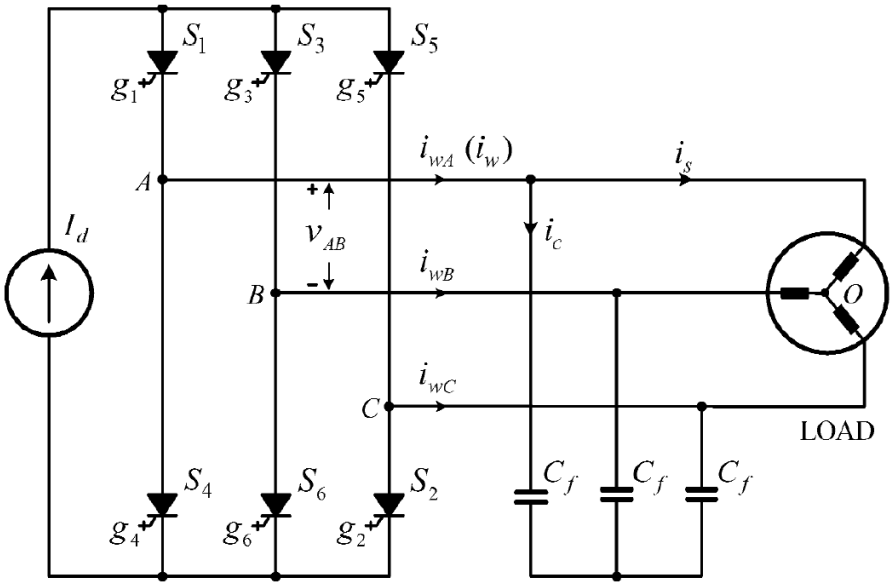


*Fig. 3-7 A PWM Current Source Inverter* [23]

In general, the Current Source Inverter requires a capacitive load at its output (capacitors) to assist the commutation of the switches. Besides, the output capacitors act as harmonics' filter that improves the load current and voltage waveforms. The DC current source can be achieved from a closed loop-controlled PWM current source rectifier, and it can be smoother and more continuous using a DC choke in series with the voltage source, as shown in Fig. 4-8.

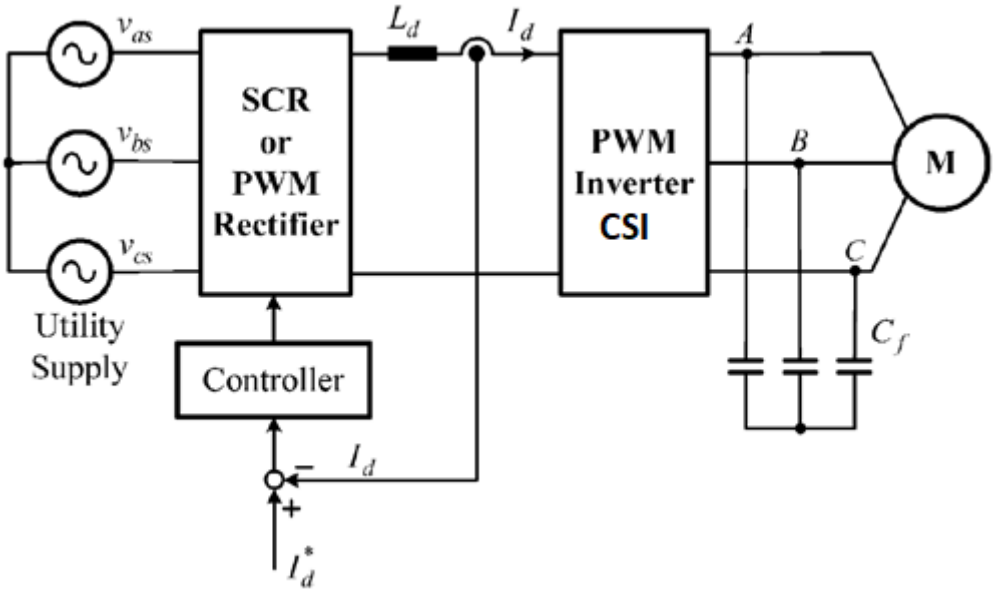


*Fig. 3-8 Realization of the DC current source in PWM CSI* [23]

Pulse Width Modulated Current Source Inverter has the following characteristics:

1- Simple structure: switches with reverse blocking capability are used, thus they do not require the antiparallel freewheeling diodes.
2- Motor friendly waveforms: the output waveforms of the PWM CSI are much closed to the sinusoidal shape. That is because the high $^{dv}/_{dt}$ problem existing in the Voltage Source Inverters VSIs does not exist in CSIs.
3- Reliable short-circuit protection: since the DC choke in the input side limits the rise rate of the short circuit current, which gives more time for protection devices to trip accordingly.
4- Limited dynamic performance: since the DC current cannot be changed instantaneously during transient (drawback).

### 3.2.2 Parallel Current Source Inverters

For high power applications, a parallel topology of the PWM CSI can be used. Also, series switches instead of each individual switch can be used, as shown in Fig. 3-9. Both inverters are sharing the same output capacitor filter, but each one has its own series DC choke [23], [35], and [36].

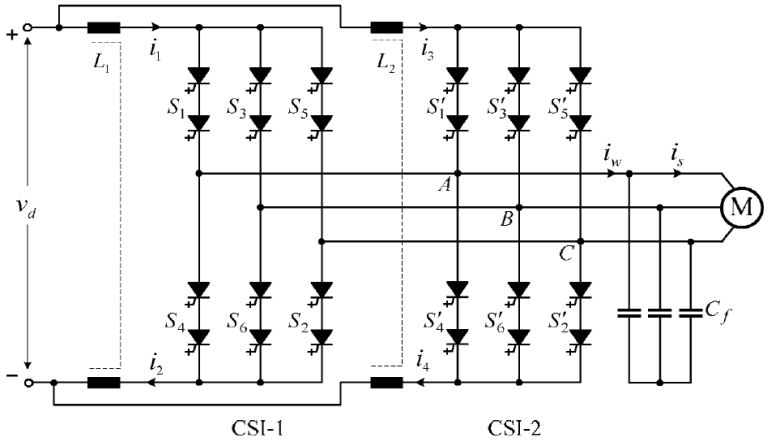


*Fig. 3-9 Parallel CSIs for high power applications* [23]

Actually, this schematic has some drawbacks regarding the balance of the DC currents [36]; (a) unequal on-state voltages of the switches, that affects the balance of the DC current and needs more advanced control techniques (b) Any time variation occurring between the gate signals of both inverters' switches will affect the DC current balance during both steady state

and transients modes (c) tolerance between DC chokes for each inverter. Nonetheless, Space Vector Modulation (SVM) may be used to solve the problem of the DC current balance [35], [36].

### 3.2.3 Load-Commutated Current Source Inverter (LC CSI)

It is a very well-known Current Source Inverter topology [37]. It has a relatively simple structure and capable of very high-power levels. Besides, its manufacturing cost is low since it depends on the SCR switches in its structure. A DC choke is used in the input side to smooth the DC current. Fig. 3-10 shows a Load Commutated Current Source Inverter for a synchronous motor drive.

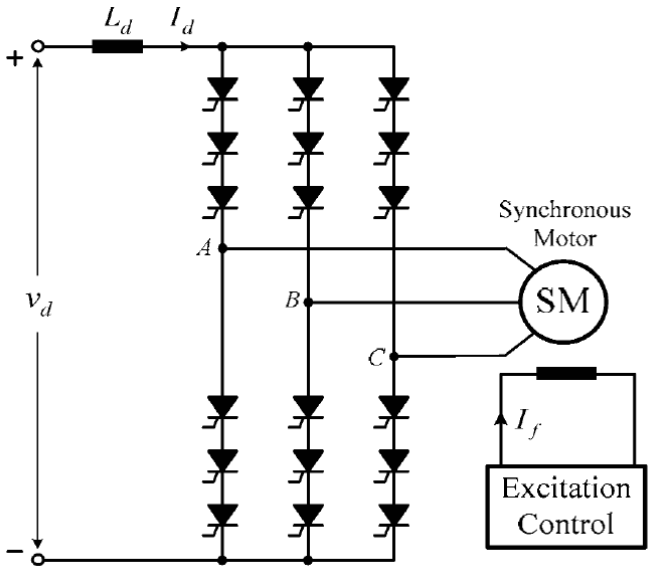


*Fig. 3-10 LCI for SM drive* [23]

SCR switches are used in the LC CSI, instead of the Gate Commutated Thyristor (GCT) switches that are used in the PWM CSI. That means, they are not capable to turn off by themselves. They can be naturally commutated by the load voltage with a leading power factor. That justifies why it is used extensively in the synchronous motor drives [23]. Since it's easy to operate the SM at a leading power factor by adjusting the excitation current. A concern appears at the low speeds of the motor, where the induced EMF value is not enough to commutate the SCRs, in this case the commutation is done using front-end SCR rectifiers [37]. That causes a low dynamic performance of the LC CSI. Besides that, the power losses in the motor are large due to the large amounts of harmonics in the stator current [38].

### 3.2.4 Boost-Type CSI

This type of Current Source Inverter is divided into two categories: a negative polarity and a positive polarity Boost Current Source Inverters [7].

#### 3.2.4.1 Negative Polarity Boost-type CSI

It is proposed to be used in the photovoltaic systems to improve the power quality, reduce the current harmonics and decrease the switching frequency. Besides, this topology can complete the maximum power point tracking [39][40]. Fig. 3-11 shows the inverter topology.

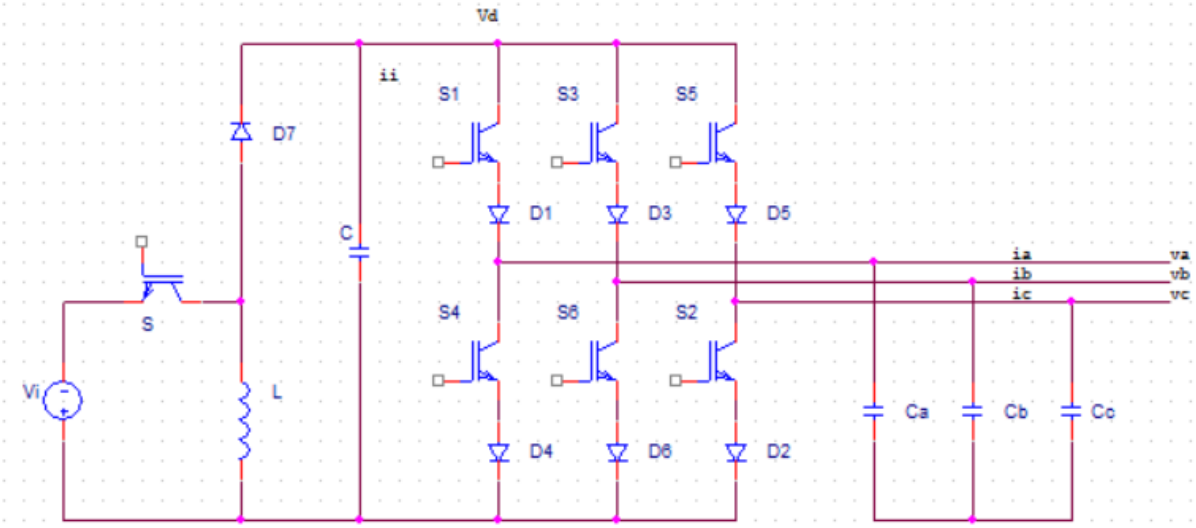


*Fig. 3-11 Negative Polarity Boost-Type CSI*

It's noticed from Fig. 3-11 that; the input voltage is a negative polarity source. Components $v_i$, L, C and the switch "s" form a DC-DC boost converter. The voltage $v_d$ can be more or equal to the input voltage. Actually, the circuit from $v_d$ to $(v_a, v_b, v_c)$ is a voltage source inverter.

#### 3.2.4.2 Positive Polarity Boost-type CSI

It doesn't differ too much from the topology of the negative polarity CSI. Fig. 3-12 shows the topology for the positive polarity boost-type CSI. Components $v_i$, L, C and the switch "s" form a DC-DC boost converter. The voltage $v_d$ can be more or equal to the input voltage. Actually, the circuit from $v_d$ to $(v_a, v_b, v_c)$ is a Voltage Source Inverter [7].

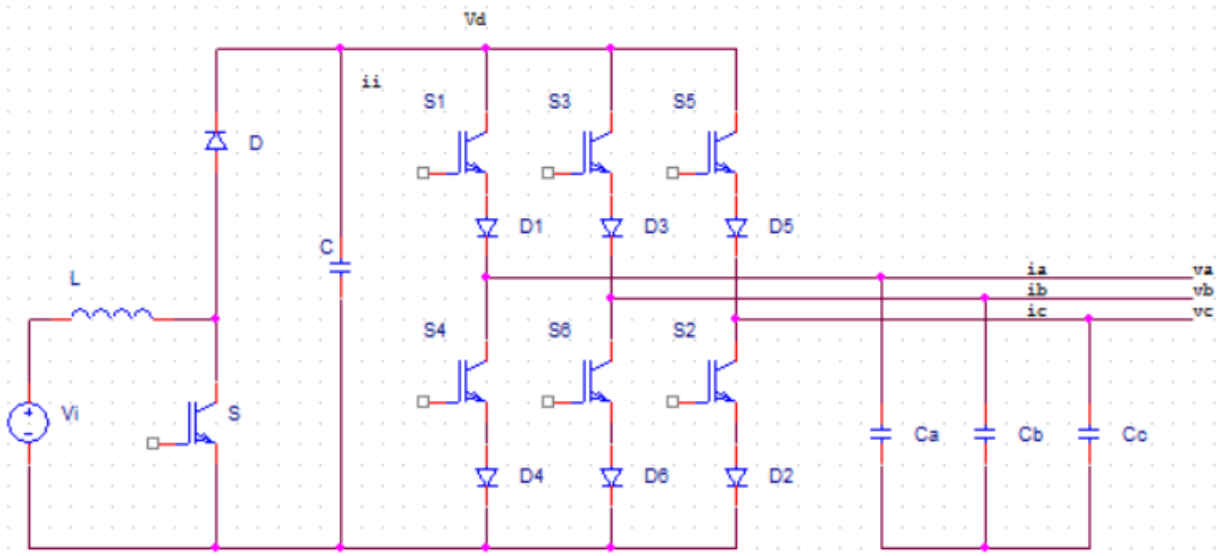


*Fig. 3-12 Positive Polarity Boost-Type CSI*

### 3.2.5 LC CSI

This topology is derived from the full bridge Current Source Inverter. The LC filter has boosting characteristics, which means that the output voltage can be higher than the input voltage. Fig. 3-13 shows the structure of the LC CSI.

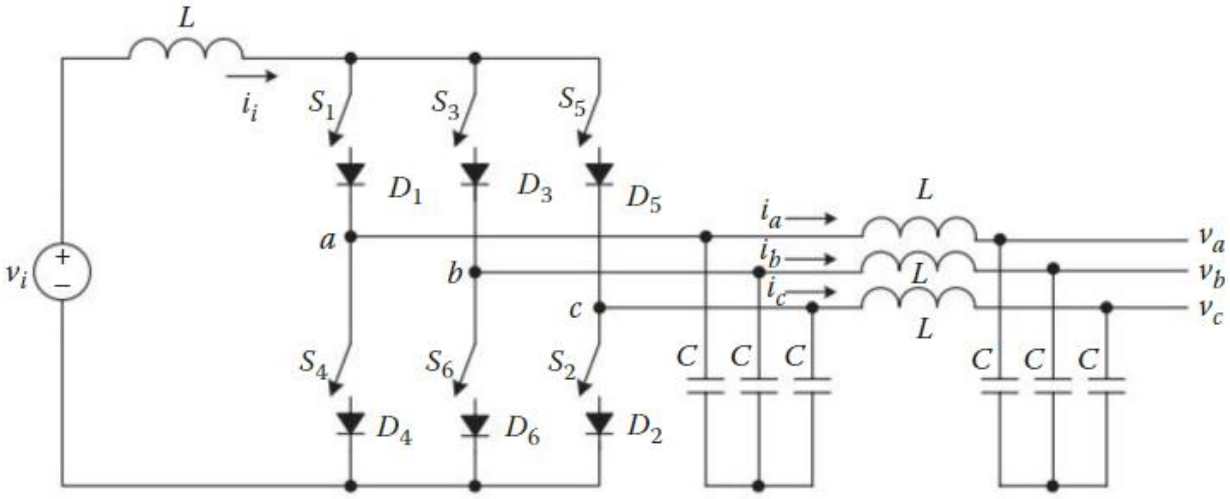


*Fig. 3-13 LC Current Source Inverter*

Many advanced control processes were proposed for the LC CSI [41][42]. Most of these control processes depend on the Space Vector Modulation (SVM).

### 3.2.6 Multi-Level Current Source Inverters (MCSIs)

Using a series inductor with the voltage source to get the required Current Source in the Current Source Inverters was one of the most important reasons behind the low popularity of them. They have higher conduction losses and so, a low efficiency inverter compared to capacitors used in the voltage source inverters. However, this problem is to be solved following the development of Superconducting Magnetic Energy Storage (SMES) technologies. In addition, the need for the series blocking individual diode with the switching device has been eliminated by the recently produced Reverse Blocking Insulated Gate Bipolar Transistor (RB-IGBT). That makes the use of Current Source Inverters more usable in high power applications [43].

Many Multi-Level Current Source Inverter topologies are proposed in literature. Each topology has its own applications, advantages and drawbacks. Here are the most CSIs that have been discussed and studied by researchers in the last few years:

1- Dual PWM CSI [1], [44]
2- Embedded Multi-Level CSI [34]
3- Two-Stage Multi-Level CSI [34]
4- Cascaded Multi-Level CSI [43]
5- Single Rating Inductor Multi-Level CSI [45]
6- Back to Back Multi-Level CSI [46], [47]
7- Reduced Count Switch Multi-Level CSI [48]
8- Parallel Inductor Multi-Level CSI [49]

#### 3.2.6.1 Dual PWM Current Source Inverter

In some references, it is called parallel PWM Current Source Inverter [1]. It is formed by paralleling two or more standard PWM Current Source Inverters. Fig. 3-14 shows the three-level topology of this type of inverters. The main concept of this inverter is to equally share the AC current $i_o^{abc}$ among the standard topologies $\left({i_o^{abc}}/{2} = i_{o1}^{abc} = i_{o2}^{abc}\right)$. That means that, both current sources must be equal $i_{i1} = i_{i2}$. It can be achieved by using two separate DC current sources or by properly controlling the gate signals of switches. Actually, this is the main challenge in this type of inverters, and many solution were presented to solve this problem [1]. It is common to use the sinusoidal pulse width modulation technique for the dual Multi-Level Current Source Inverters.

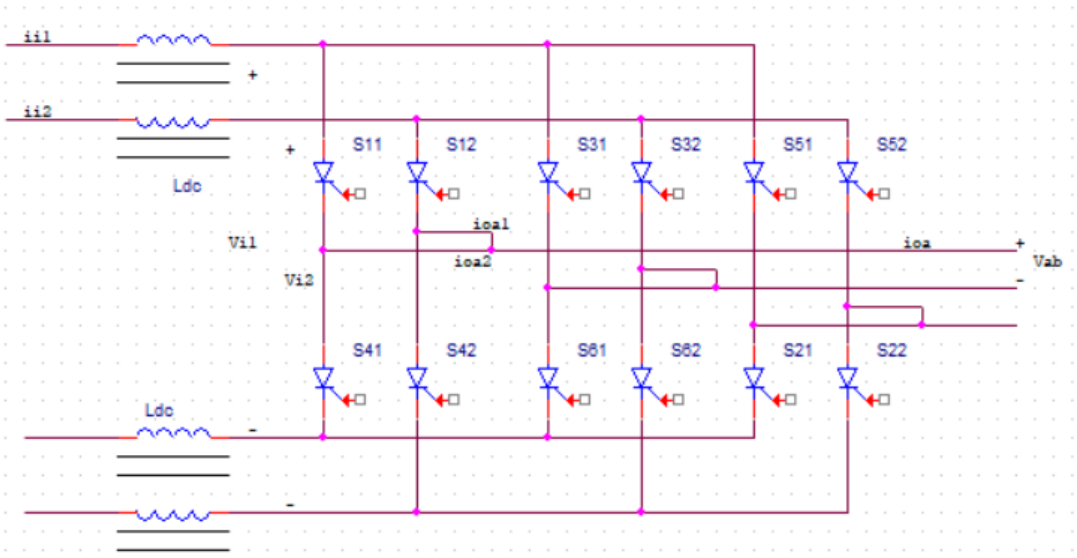


*Fig. 3-14 Three-level Dual PWM Current Source Inverter*

### 3.2.6.2 Embedded Multi-Level CSI

It is one of the simplest topologies for the Multi-Level Current Source Inverters. It can be generalized easily for any number of levels. In [50], two switching methods were introduced to control the gate signals of the switches, symmetrically and asymmetrically. Fig 3-15 shows the 5-level topology for the embedded current source Multi-Level Inverter.

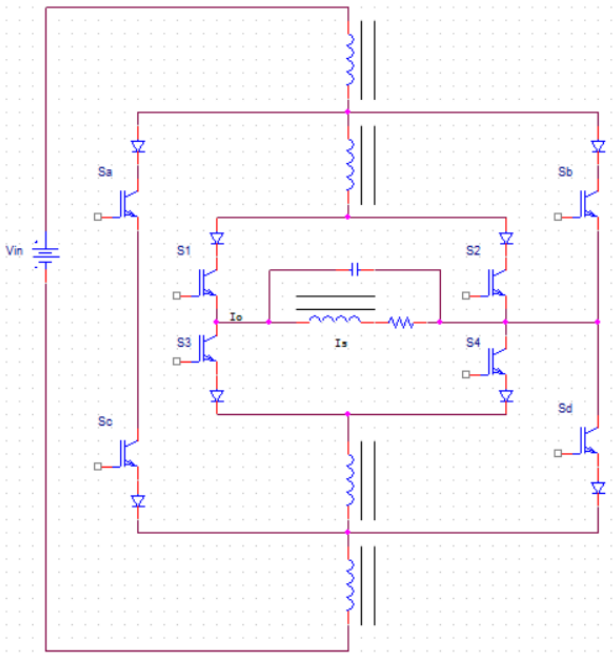


*Fig. 3-15 Five-level Embedded Multi-Level CSI*

### 3.2.6.3 Two-Stage Multi-Level CSI

Different topologies that have mini differences were proposed for the Two-Stage Current Source Multi-Level Inverters [34], [51]. Basically, all proposed topologies consist of two different stages, the first one is a power boosting stage (boost converter), whilst the other is a DC to AC conversion stage (Current Source Inverter), as shown in Fig 3-16. Actually, the two-stage power conversion system means that, the power will be transmitted twice, so the power losses in this case is a main concern. In some cases where the DC input is more than the AC output voltage, the pre-stage is not necessary to be used. That may improve the efficiency of the system and reduce power stress of the boosting stage [51]. Fig 3-17 shows the semi-two-stage Multi-Level based on the last idea.

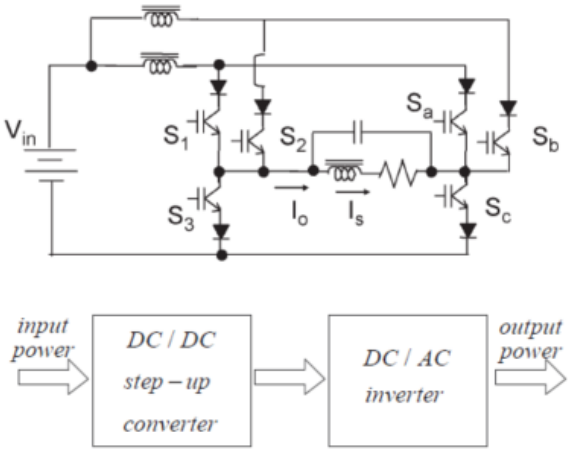


*Fig. 3-16 Two-stage Multi-Level CSI* [34]

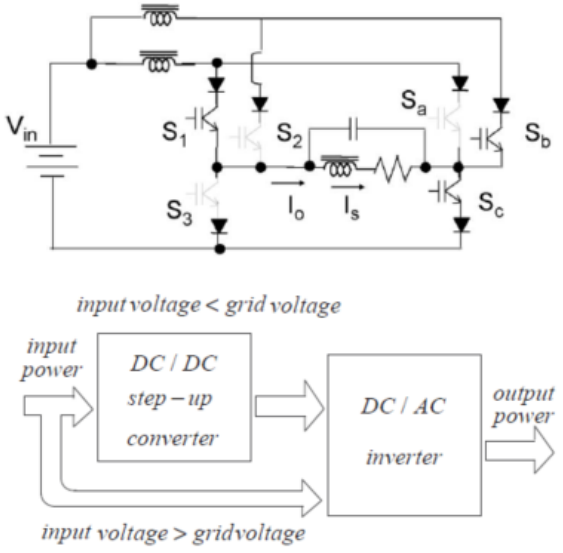


*Fig. 3-17 Semi-two-stages Multi-Level* [34]

### 3.2.6.4 Cascaded Multi-Level CSI

In this topology, the inverter consists of parallel connected CSI modules operating at a very low switching frequency [43]. The output current levels equal 2n+1 where n is the inverter modules. Each module has its own input source. Input sources may be equal or unequal. That makes it good to be used in photovoltaic systems. Moreover, this topology is an efficient structure in terms of filtering and sensors. The output current injected into the AC grid is a high-quality sinusoidal waveform. However, in addition to the pulse width modulation technique, this inverter needs a synchronization controller to synchronize the output current exactly with the grids', as shown in Fig 3-18. The structure of the inverter consists of cascaded determined number of PV arrays (or DC voltage source). Each DC sources is connected with an in-series high-value inductor to maintain the current source. The current source is connected with a half bridge converter. The output of the converter consists of a capacitance filter and a step-up transformer. A coupling L-filter is introduced to connect between the converter and the grid.

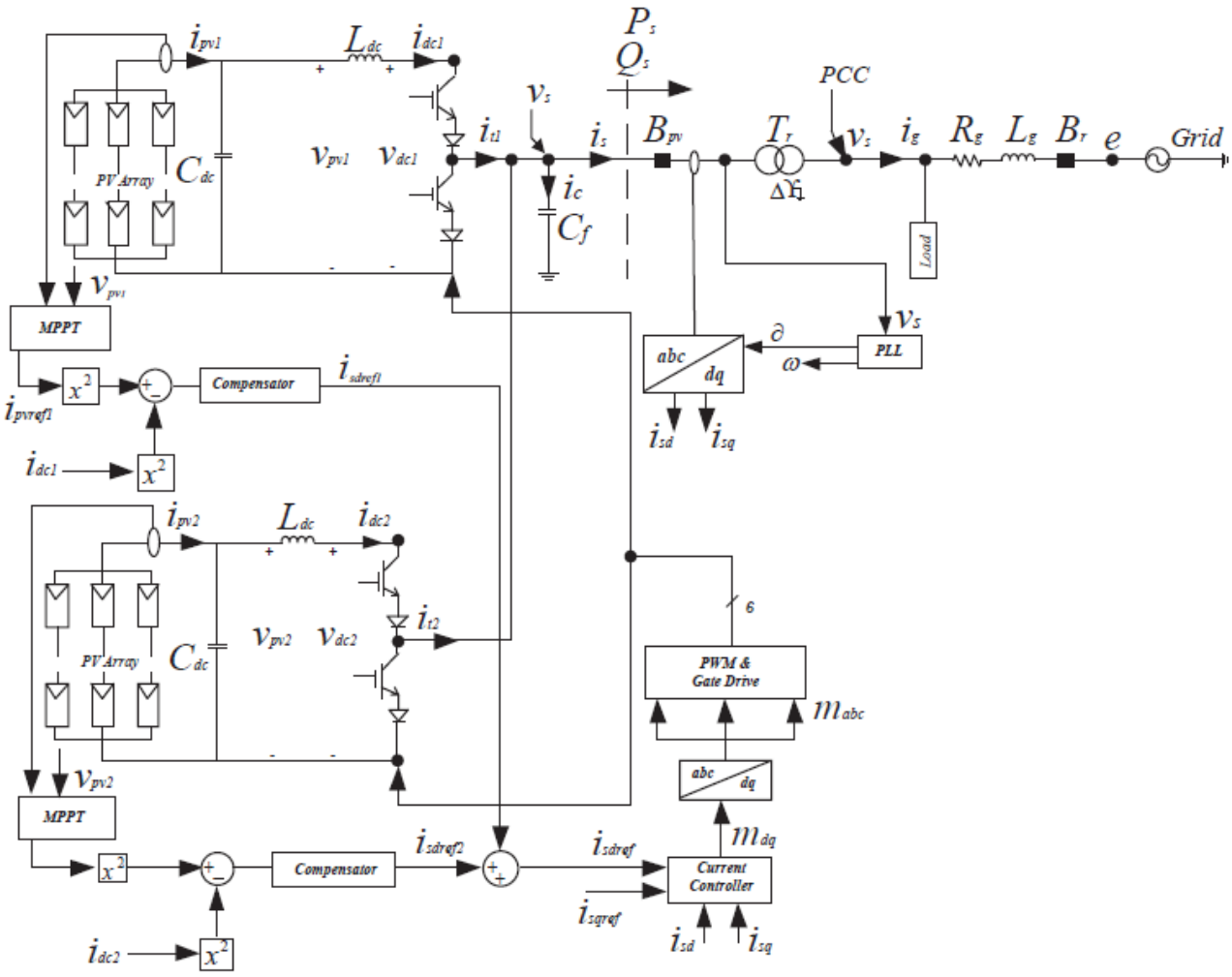


*Fig. 3-18 Parallel Multi-Level CSI with controllers in PV applications* [43]

### 3.2.6.5 Single Rating Inductor Multi-Level CSI

In this type, the topology of the inverter consists of just one input source and n-identical modules of full bridge DC to AC inverters, as shown in Fig 3-19. All inductors of every module should carry the same amount of current [52]. Identical modules and modularity of this inverters make it very easy to be manufactured and assembled. Also, in this topology, the number of levels in the output current equals 2n+1, where n is the number of the full bridge DC to AC inverters. In some cases where there is an imbalance in the output three phase currents due to the unmatched components, unequal on-state characteristics of the switches, modulation errors or nonlinear loads, a balanced controlling process must be introduced [45], [47].

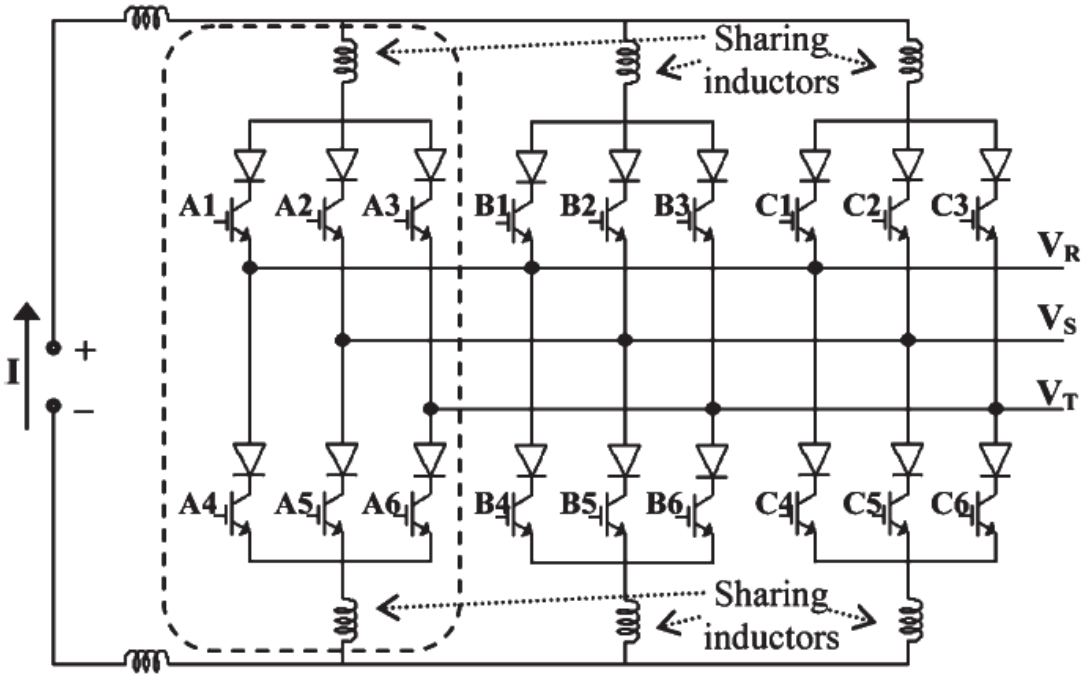


*Fig. 3-19 Single Rating Inductor Multi-Level CSI* [52]

In [45] a mathematical model is derived for the Single-Rating Inductor Multi-Level. To get a high-speed data processing, variable bit accuracy, fault tolerant architectures and easily scalable design, the Field Programmable Gate Array (FPGA) is used to implement the control process of the inverter. In addition to these advantages, one of the most powerful advantages of an FPGA is the ability to compute all the converter control blocks in parallel, saving time and increasing reliability [45], [52].

### 3.2.6.6 Back to Back Multi-Level CSI (BTB CSI)

It is a full bridge three phase Current Source-based Inverter. Composed of parallel modules back to back full bridge Current Source Inverters. Fig 3-20 shows the five-level topology of this inverter. It is introduced to be used in the motor drives applications due to its high output efficiency. Besides, it has a high boosting capabilities [22], [46].

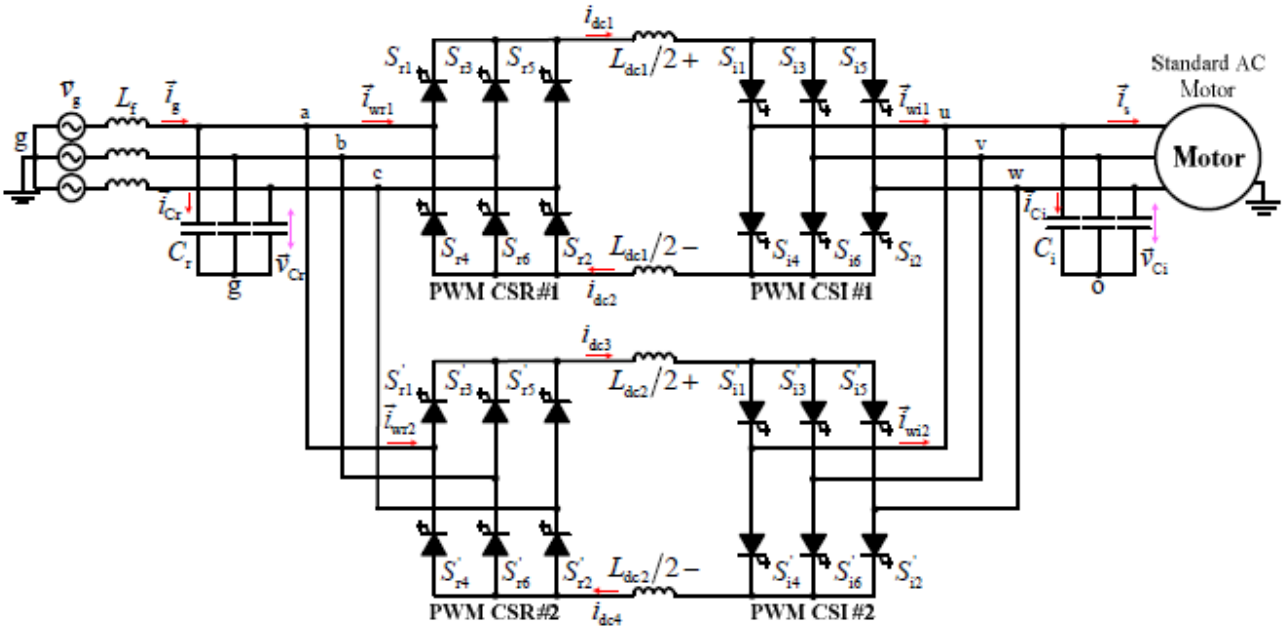


*Fig. 3-20 Five-levels Back to Back Multi-Level CSI* [46]

In addition to the pulse width modulation, selective harmonic elimination and space vector modulation, a new technique of control is used to control this BTB CSI, which is the Model Predictive Control (MPC). It has appealed the attention from researchers in power electronics control field [53], [54]. As it was illustrated previously in many topologies of Current Source Inverters, if it is required to gain high power ratings at the output, two or more switches may be used to replace each individual switch in the main topology of the inverter [23].

### 3.2.6.7 Reduced Count Switch Multi-Level CSI

It is basically based on modular cells. The topology of the reduced count switch Multi-Level Inverter is built by the parallel connection of two-switch modules, as shown in Fig 3.21. The operation of the inverter depends mainly on the value of the DC input current of the two modules, and it is divided into two types: symmetric, which means equal input DC current supplies, and asymmetric, which means unequal input DC current supplies. The main advantages of this topology are the reduced number of switching devices, DC supplies and lower implementation cost due to common-emitter connection of the IGBTs compared to

traditional topologies [48]. Switches used are unidirectional current switches that can be implemented by a single diode-less IGBT (an IGBT with a reverse blocking capability) or an IGBT/diode with a series connected diode.

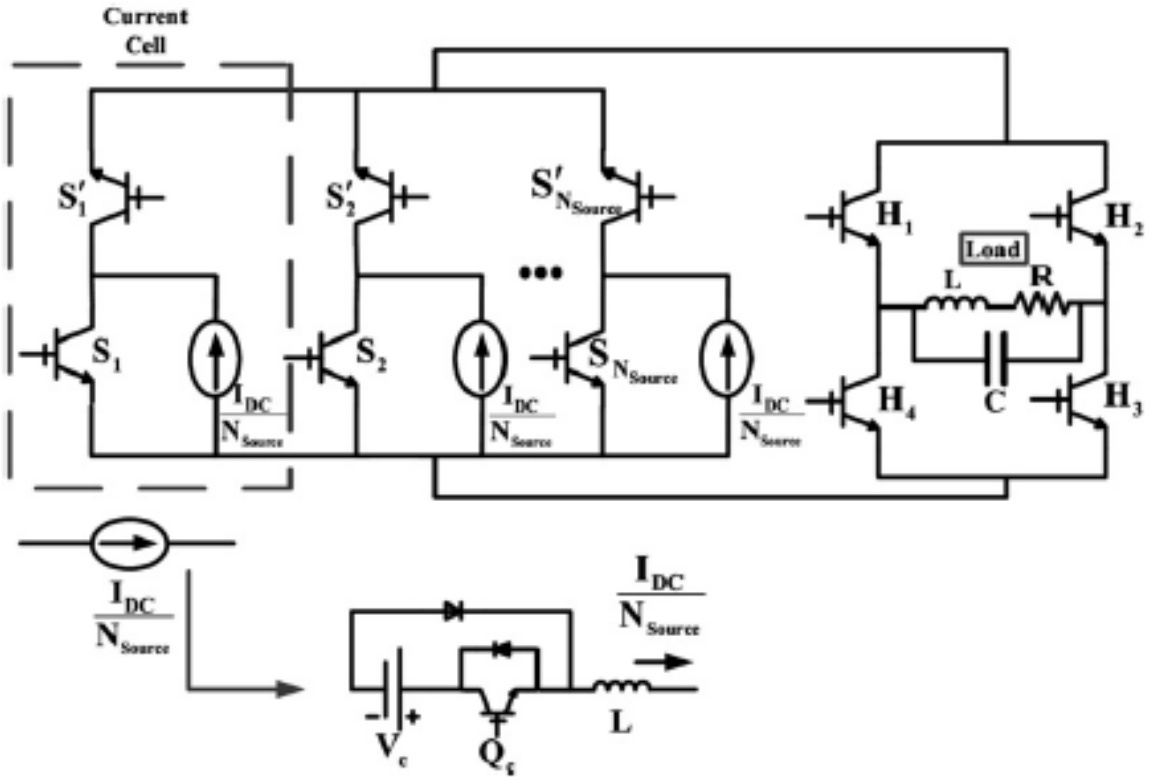


*Fig. 3-21 Reduced count switches Multi-Level CSI* [48]

### 3.2.6.8 Parallel Inductor Multi-Level CSI

It is a modified version of the parallel Multi-Level Current Source Inverter as shown in Fig 3-22. It introduces an energy recovery scheme that provides a major path to release its stored energy and to enable the balance of the sharing inductor currents. In addition, a chopper circuit with a smaller inductor size is employed to replace the large and bulky input DC link inductor, that is used in other topologies of Multi-Level Inverters [49].

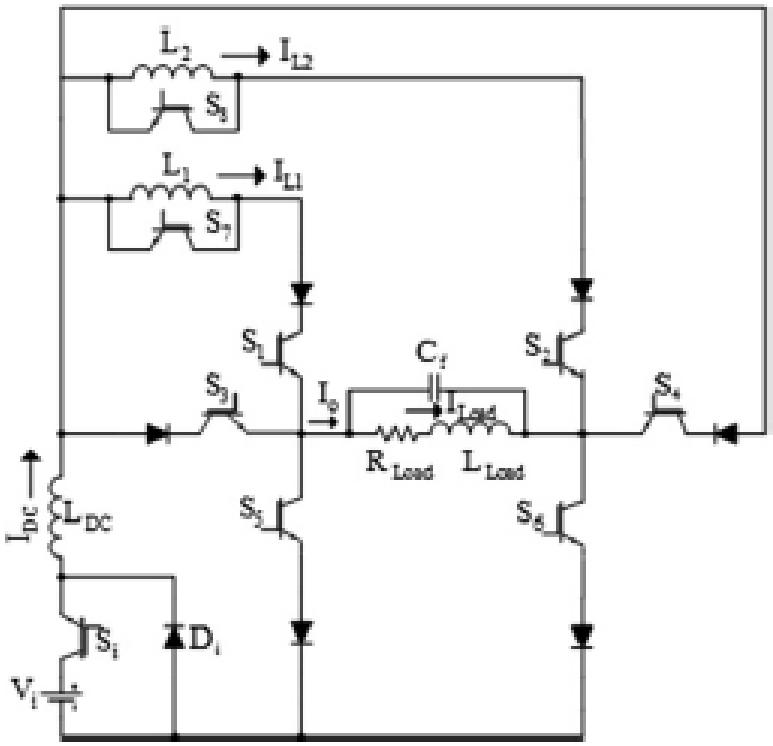


*Fig. 3-22 Five-levels Parallel Inductor Multi-Level CSI* [49]

By now, the remaining types of DC to AC converters are the Hybrid Multi-Level Voltage Source Inverters and Hybrid Multi-Level Current Source Inverters. These inverters will be discussed by details in Chapter 4.

# Chapter 4. Multi-Level Inverters Modulation Techniques

One of the most critical control processes for the Multi-Level Inverter is the modulation technique used. There are many modulation techniques suggested for two-level DC-to-AC inverters such as the square wave strategy, harmonic elimination method, Sinusoidal Pulse Width Modulation (SPWM), sinusoidal pulse width modulation with third harmonic injection method and space vector modulation (SVM) method.

In Multi-Level and Hybrid Multi-Level Inverter, other modulation methods were proposed, depending on the type of the inverter, number of switches and control process complexity. In addition to the aforementioned methods, other methods were proposed and tested. Here are the most popular modulation techniques used to produce gate signals in the Multi-Level and Hybrid Multi-Level Inverters:

1- Level-Shift PWM (Level Deposition)
2- Phase Shift PWM
3- Phase Deposition
4- Space Vector Modulation (SVM)

## 4.1 Sinusoidal Pulse Width Modulation

First of all, the Pulse Width Modulation method is a method to generate pulses that are used to control the gate of the switching devices (switches) of the inverter. It depends on a comparison between two main signals. The first one is the control signal (modulating signal), $V_c$, and the other one is a triangular signal, $V_{tri}$. The interval during which the control signal is greater than the triangular signal, the output is 1, and the interval where the control signal is less than the triangular one, the output is zero.

Since the output of the inverter is desired to be a sinusoidal waveform, it is recommended to use the sinusoidal control signal in the modulation process. This makes the output signal closer to the sinusoidal shape, and has less harmonic components, making the design of the filter easier and cheaper.

There are two important indices that describe the modulation process, one is corresponding to the amplitude, which is the modulation index ($M_a$) and is define as:

$$M_a = \frac{\hat{V}_C}{V_\Delta} \tag{4.1}$$

where $\hat{V}_C$ is the peak of the modulating signal, whilst $V_\Delta$ is the value of the triangular signal

The other index is corresponding to the frequency and is called normalized carrier frequency, $M_f$.

$$M_f = \frac{f_\Delta}{f_c} \tag{4.2}$$

Where, $f_\Delta$ is the frequency of the triangular signal and $f_c$ is the frequency of the control signal.

For more clarification, Fig. 4-1 shows the power topology of a half-bridge Voltage Source Inverter. Moreover, the sinusoidal pulse width modulation process is illustrated in Fig. 4-2.

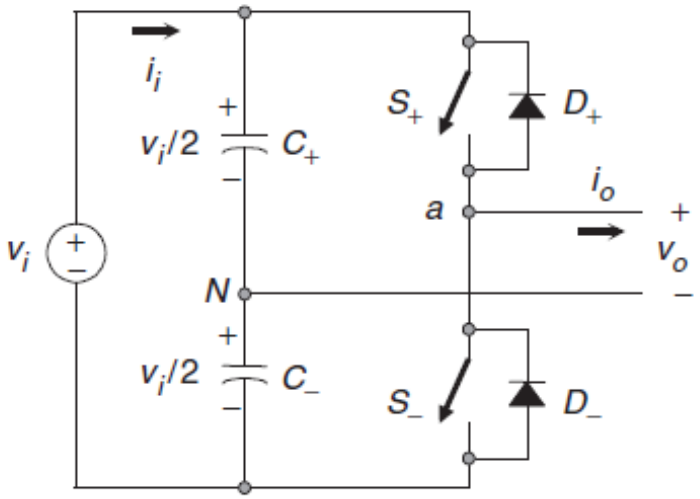


*Fig. 4-1 Single phase half-bridge VSI* [1]

For inverters with more than one leg, like the full-bridge inverter, shown in Fig. 4-2, there are two schemes which can be used to implement the sinusoidal pulse width modulation; unipolar and bipolar schemes. In the bipolar scheme, just one sinusoidal modulating signal is used. In this case, the on-state in switch S+ in the half-bridge corresponds to both switches $S_{1+}$ and $S_{2-}$ being in the on-state in the full-bridge configuration in Fig 4-3. Similarly, $S_-$ in the on-

state in the half-bridge corresponds to both switches $S_{1-}$ and $S_{2+}$ being in the on-state in the full-bridge configuration.

But, in the unipolar scheme, two sinusoidal modulating signals ($v_c$ and $-v_c$) are used. Each inverter leg is controlled by a separate control signal, independently. Both control signals have the same magnitude, but they are shifted by $180^{\circ}$. Implementing the unipolar scheme doubles the effective switching frequency at the output, without additional switching losses, but of course it needs an extra control signal.

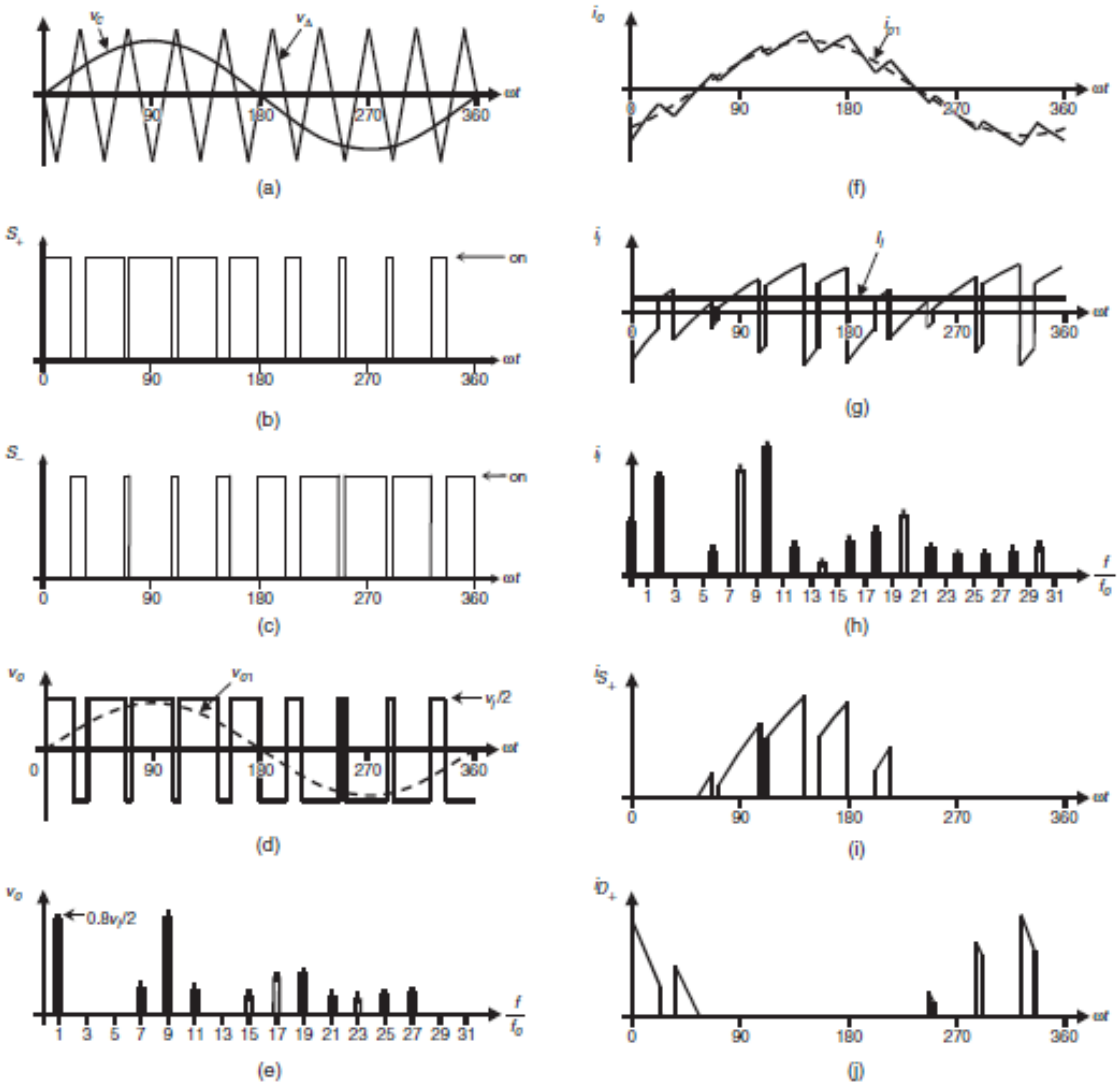


*Fig. 4-2 The half-bridge VSI. Ideal waveforms for the SPWM ($M_a$= 0.8, $M_f$ = 9): (a) carrier and modulating signals; (b) switch S+ state; (c) switch S− state; (d) AC output voltage; (e) AC output voltage spectrum; (f) AC output current; (g) DC current; (h) DC current spectrum; (i) switch S+ current; and (j) diode D+ current* [1]

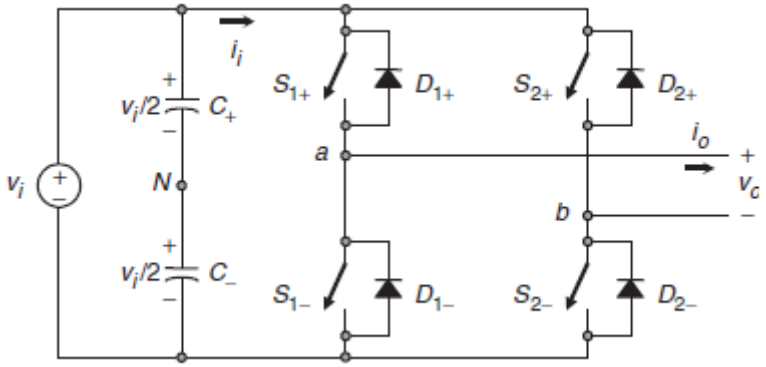


*Fig. 4-3 Single phase full-bridge inverter* [1]

## 4.2 Phase-Shifted Multicarrier Modulation

In the phase-shifted modulation method, all triangular signals have the same frequency and the same peak to peak amplitude, but they are phase-shifted by a value $\emptyset_{cr}$ given in eq. 4.3. The modulating signal is also a sinusoidal signal (3 sinusoidal signals are needed for 3 phase output).

$$\emptyset_{cr} = 360/(m-1) \tag{4.3}$$

where m is the number of levels in the output voltage [23], [45], [49].

## 4.3 Level-Shifted Multicarrier Modulation

In this scheme, the carrier modulating signals are vertically disposed such that the bands they occupy are contiguous [44], [48]. There are three implementation ways for the level-shifted modulating signals: a) In-phase disposition (IPD), where all carriers are in phase, b) Alternative phase opposite disposition (APOD), where all carriers are alternatively in opposite disposition, and c) Phase opposite disposition (POD), where the carriers above zero are in phase and which are below zero are in opposition [1], [55]

There are more other modulation techniques that will be discussed later in other sections of this thesis. Fig. 4-4 shows the most commonly used methods of modulation technique [56].

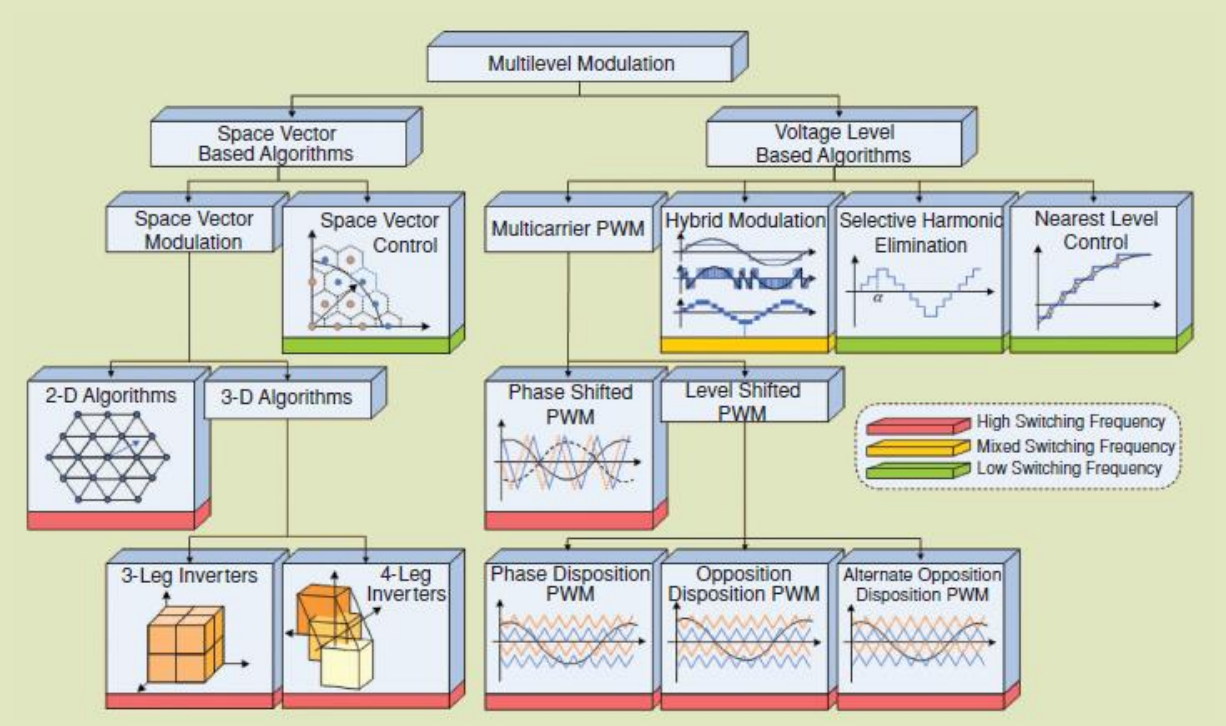


*Fig. 4-4 Classification of Modulation techniques for Multi-Level Inverters* [56]

## 4.4 Hybrid Multi-Level Inverter Analysis

As it was shown in Chapter 2, there are a lot of Hybrid Multi-Level Inverter topologies that are widely classified into voltage source Hybrid Multi-Level Inverters and current source Hybrid Multi-Level Inverters. In this chapter, just one type of inverters is chosen as a first basic step for other types in the future work. The sample Hybrid Multi-Level Voltage Source Inverter which is to be analyzed is the Asymmetric Trinary Hybrid Multi-Level Inverter (ATHMLI). THMLI has a simple structure, based mainly on the H-bridge cells. Therefore, the property of structure modularity is still valid. However, the isolated DC source for each H-bridge cell has a different value. That makes it perfect to be implemented in PV application, where it is possible to have different values of DC voltages very easily.

### 4.4.1 Asymmetrical Hybrid Multi-Level Inverter (AHMLI)

It is a topology derived from the cascaded H-bridge Multi-Level Inverter (H-bridge based inverter). As discussed in Chapter 2, the cascaded H-bridge inverter has to be provided with separate DC voltage source for each module in the inverter topology depending on the number of desired levels at the output. The traditional topology must have equal input DC voltage sources, and in some cases where the DC link capacitors are used as input for the inverter, the balancing of input voltage creates a challenge.

One of the derived hybrid inverters based on the H-bridge inverter is the Asymmetrical Hybrid Multi-Level Inverter (AHMLI). It has the same topology of the traditional H-bridge inverter, but the input voltage sources are not equal for each module, as shown in Fig. 4-5.

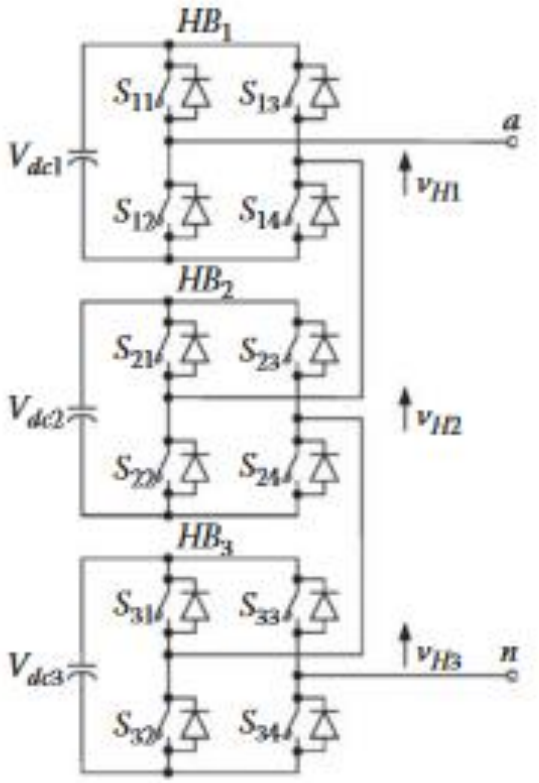


*Fig. 4-5 Asymmetrical Hybrid Multi-Level Inverter (AHMLI)* [7]

### 4.4.1 Asymmetric Trinary Hybrid Multi-Level Inverter (THMLI)

The Trinary Hybrid Multi-Level Inverter is a special topology of the Asymmetrical HMLI. The values of the input voltage sources for each H-bridge module is determined following a specific formula in eq. (4.4):

$$V_{dci} = 3^{h-1} * E \tag{4.4}$$

where h is the order of the H-bridge in the THMLI. Therefore, in the three phase THMLI, the DC input values will be [7]:

$$V_{dc1} = E, \qquad V_{dc2} = 3E, \qquad V_{dc3} = 9 * E \tag{4.5}$$

Fig. 4-6 shows the general n-level single-phase THMLI. It consists of h-HB modules that are connected in series. The number of levels in the output voltage is $3^h$ [7].

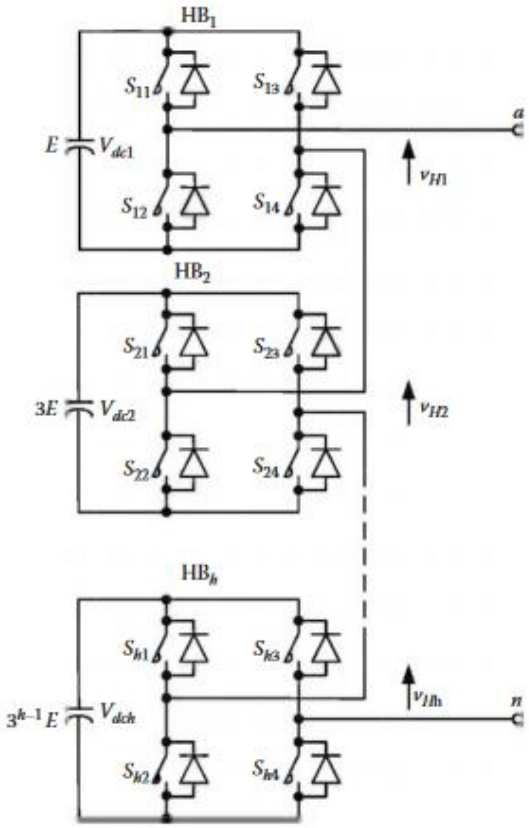


*Fig. 4-6 Single-Phase THMLI Topology* [57]

Table 4-1 shows the relationship between the input voltage of a single HB module ($v_{dci}$) and the output voltage ($v_{Hi}$).

*Table 4-1 Relationship between the input and output voltages of a single HB module in the THMLI*

| $\boldsymbol{F_i}$ | $v_{Hi}$ | $S_{i1}$ | $S_{i2}$ | $S_{i3}$ | $S_{i4}$ |
|---|---|---|---|---|---|
| **1** | $V_{dci}$ | 1 | 0 | 0 | 1 |
| **-1** | $-V_{dci}$ | 0 | 1 | 1 | 0 |
| **0** | 0 | 1 | 1 | 0 | 0 |
| **0** | 0 | 0 | 0 | 1 | 1 |

where, $F_i$ is the switching function used to relate the output and input voltages of the HB-module, as given by eq. (4.6)

$$v_{Hi} = F_i * V_{dci} \tag{4.6}$$

For the total value of the output voltage for the single phase THMLI ($v_{an}$), the outputs of all HB-modules are added to each other:

$$v_{an} = \sum_{i}^{h} v_{Hi} \tag{4.7}$$

Using eq. (4.6)

$$v_{an} = \sum_{i}^{h} F_i * V_{dci} \tag{4.8}$$

Using eq. (4.4)

$$v_{an} = \sum_{i}^{h} F_i * 3^{i-1} * E \tag{4.9}$$

The switching function $F_i$ can be generalized for the h-HB modules per phase as follows [7]:

$$F_1 = \frac{ABS(l)}{l} B_b \left( ABS(l) - \sum_{k=2}^{h} (ABS(F_k) * 3^{k-1}) \right) \tag{4.9.a}$$

$$F_2 = \frac{ABS(l)}{l} B_b \left( ABS(l) - \sum_{k=3}^{h} (ABS(F_k) * 3^{k-1}) - 1 \right) \tag{4.9.b}$$

$$F_i = \frac{ABS(l)}{l} B_b \left( ABS(l) - \sum_{k=i+1}^{h} (ABS(F_k) * 3^{k-1}) - \frac{3^{i-1} - 1}{2} \right)$$

$$F_{h-1} = \frac{ABS(l)}{l} B_b \left( ABS(l) - ABS(F_h) * 3^{k-1} - \frac{3^{h-2} - 1}{2} \right) \tag{4.9.c}$$

$$F_h = \frac{ABS(l)}{l} B_b \left( ABS(l) - \frac{3^{h-1} - 1}{2} \right) \tag{4.9.d}$$

where $B_b$, is the bipolar function that is defined as follows [7]:

$$B_b(\tau) = \left\{ \begin{array}{cc} 1 & \tau > 0 \\ 0 & \tau = 0 \\ -1 & \tau < 0 \end{array} \right\} \tag{4.10}$$

# Chapter 5. Grid-Tied PV Inverters

## 5.1 Introduction

Grid-tied PV systems supply the maximum available power to the grid. The PV system consists of the PV array, boost converter, maximum power point tracker, inverter, and output filter. Each component is discussed individually to explain its role in the whole system. Besides, the PV should supply power to grid in various condition and different variety of grid linear and non-linear loads, in a high-power quality within standards parameters and constraints.

## 5.2 Topology

The complete design of the THMLI is illustrated in Fig. 5-1. First of all, the PV array is designed and arranged to fulfill the input voltage criterion discussed in section 4.4.1. In this way, the conventional MLI is converted to HMLI using variable values of input voltages for each leg. To produce a regulated output voltage from the PV array, a boost converter is used to achieve the required value of voltage for the DC-link, which constructs the input voltage of the HMLI legs.

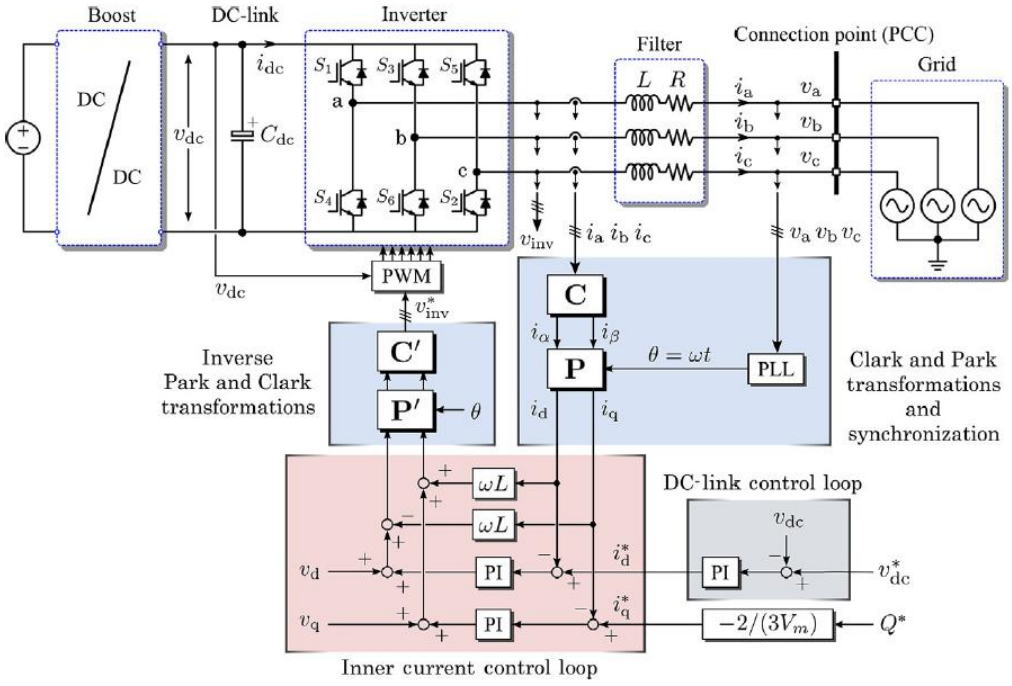


*Fig. 5-1 Complete Topology of the Grid-Tied HMLI* [58]

However, a MPPT is used to control the output voltage of the PV array and the boost converter. Under variable ambient conditions, including irradiance and temperature, the DC-link voltage must be kept constant as required in the design values even when the output load is variable [59].

## 5.3 Coupling Filter

Usually, HMLIs' outputs contain fewer harmonics than the traditional inverters. That is due to their output shape, which is similar to the staircase, thus a closer to the sinusoidal shape waveform results. However, to achieve the maximum power output quality, output harmonics must be eliminated, and the value of the Total Harmonics Distortion (THD) must be as minimum as it could be. So, a low-pass filter is required between the inverter and the grid. According to their complexity and functionality, three topologies of filters were introduced [60],[61]:

1- L filters
2- LC filters
3- LCL filters

“L” filters are very simple. They are considered as first-order filters. Nevertheless, the switching frequency must be very high to attenuate output harmonics and to produce the required output. Operating the inverter using a very high switching frequency causes the power losses to increase, and decreases its power efficiency. Besides, the required inductor will be bulky, heavy and very expensive [62].

Introducing the second-order LC filters did not cause much better output results. On the contrary, the filter design became relatively bulkier and more expensive [61]. There was a great common work in literature to go toward the third-order LCL filters design [63]–[71]. Implementing LCL filters reduces the values of the inductances and hence a more compact design and lower costs. Fig. 5-2 shows different topologies of grid-tied filters. The main drawback of the LCL is the possibility of resonance occurrence. This possibility may cause the control process of active and reactive power unstable. To overcome this problem, damping elements must be added to the LCL branches [62]. In this thesis, resistors were added.

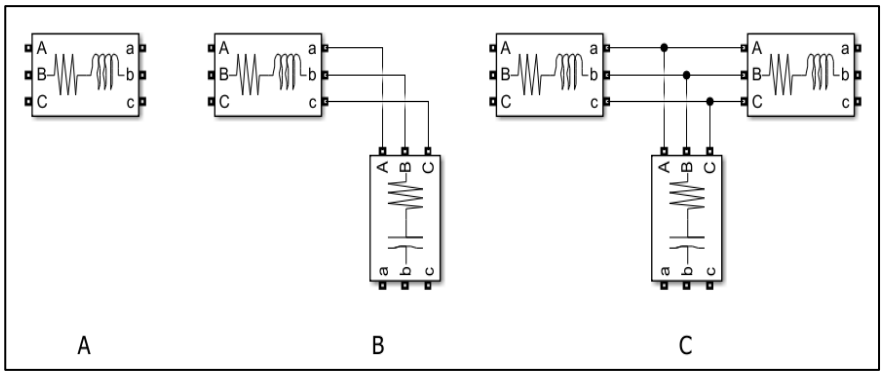


*Fig. 5-2 Grid filter different topologies, A) L filter, B) LC filter, and C) LCL filter*

## 5.4 Grid Tied PV Controllers

The main objective of the grid-tied inverters is to supply the active power to the grid with a reasonable power quality. The Total Harmonic Distortion (THD) must be within the international standard values. In addition, the grid-tied inverter should have grid-support functionalities such as reactive power injections or active power control capabilities. These requirements are demanded to avoid the adverse impact of the intermittent power injection from renewable energy sources. Therefore, the controllers of the grid-tied inverter have an important and necessary role in achieving the maximum power quality of the grid. Mainly, the

sending and receiving power between two power supplies at the coupling point, shown in Fig. 5-3 are given according to eqs. (5.1) and (5.2) [72]:

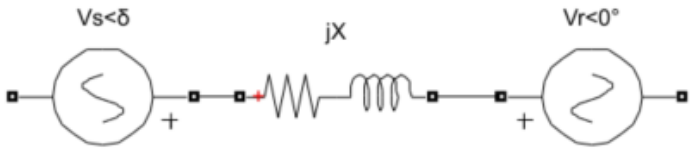


*Fig. 5-3 Power transmission between two power supplies*

$$P_r = \frac{V_s V_r}{X} \sin \delta \tag{5.1}$$

$$Q_r = V_r \frac{V_s \cos \delta - V_r}{X} \tag{5.2}$$

where,

$P_r$ is the receiving end active power.

$Q_r$ is the receiving end reactive power.

$V_r$ is the voltage value at the receiving end.

$V_s$ is the voltage value at the sending end.

X is the reactance of the line between the two sources.

δ is the phase shift between the sending and receiving side voltages.

It is obvious that, the dominant factors between both sending and receiving active and reactive power are different. The dominant factor that controls the active power is the phase shift between the sending and receiving ends. Whereas the dominant factor that controls the reactive power is the amplitude of the sending end voltage value.

# Chapter 6. Design and Modeling of THMLI

## 6.1 Introduction

The complete design of the THMLI in this chapter includes six main parts:

1- Design of the Sinusoidal Pulse Width Modulation, adopting the LS techniques.
2- Design of the PV array including the arrangement, boost converter, MPPT, and the output DC-link voltage.
3- The cascaded H-bridge cells.
4- Coupling filter.
5- Controllers.
6- Grid parameters.

## 6.2 Sinusoidal Pulse Width Modulation

The PWM modulation controller is designed to provide 6 reference signals for each leg of the inverter. Fig. 6-1 shows the model of the used PWM modulation for leg A. The switching frequency is 5,000Hz, usually it is used to be between 2kHz and 20kHz in the MLIs [73], to enhance the value of the THD. It is chosen depending on the output filter of the inverter, equipment size and the Total Harmonic Distortion required at the output current of the inverter. The reference signals for the other legs, B and C, are determined using the level shifting procedure.

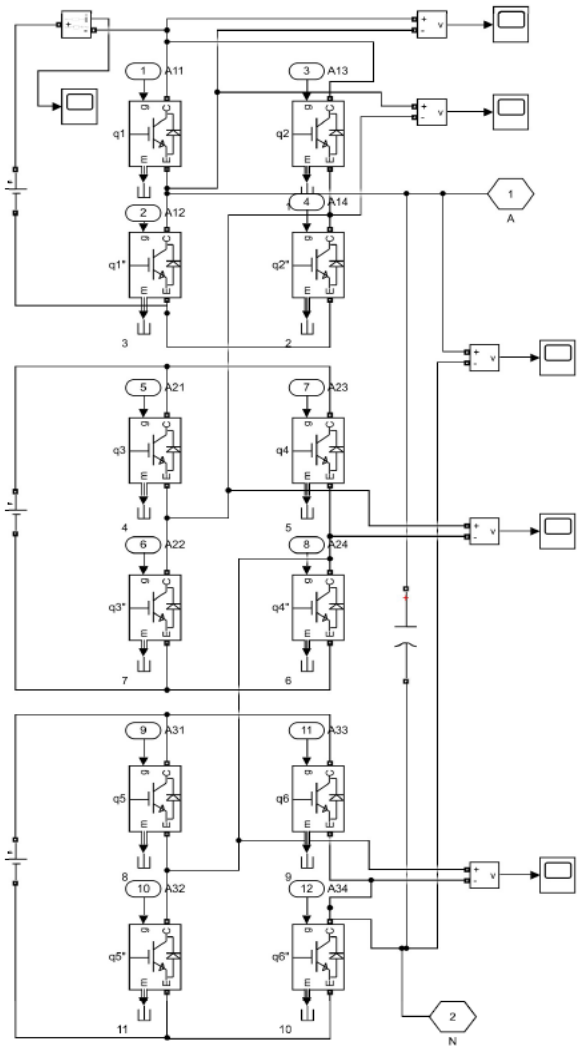


*Fig. 6-1 Phase A structure*

The modulation signals are generated within the P-Q controller at the final stage of the inverter. Fig. 6-2 shows the complete generation process of the reference signals. Fig. 6-3 shows the finals results of the triangular signal that are used to produce the gate signals of the switches.

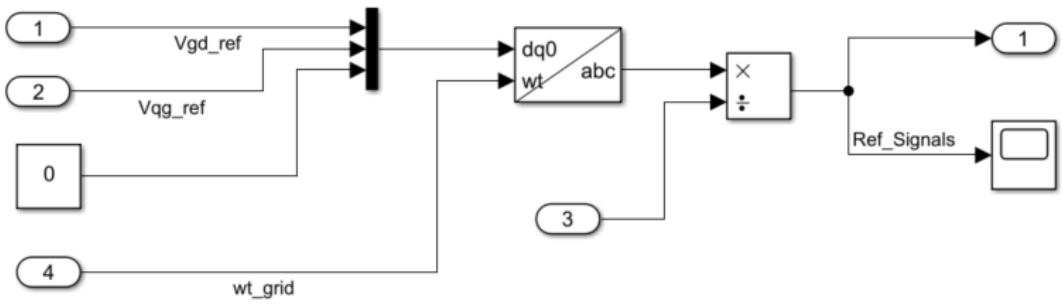


*Fig. 6-2 Generation process of the reference signals*

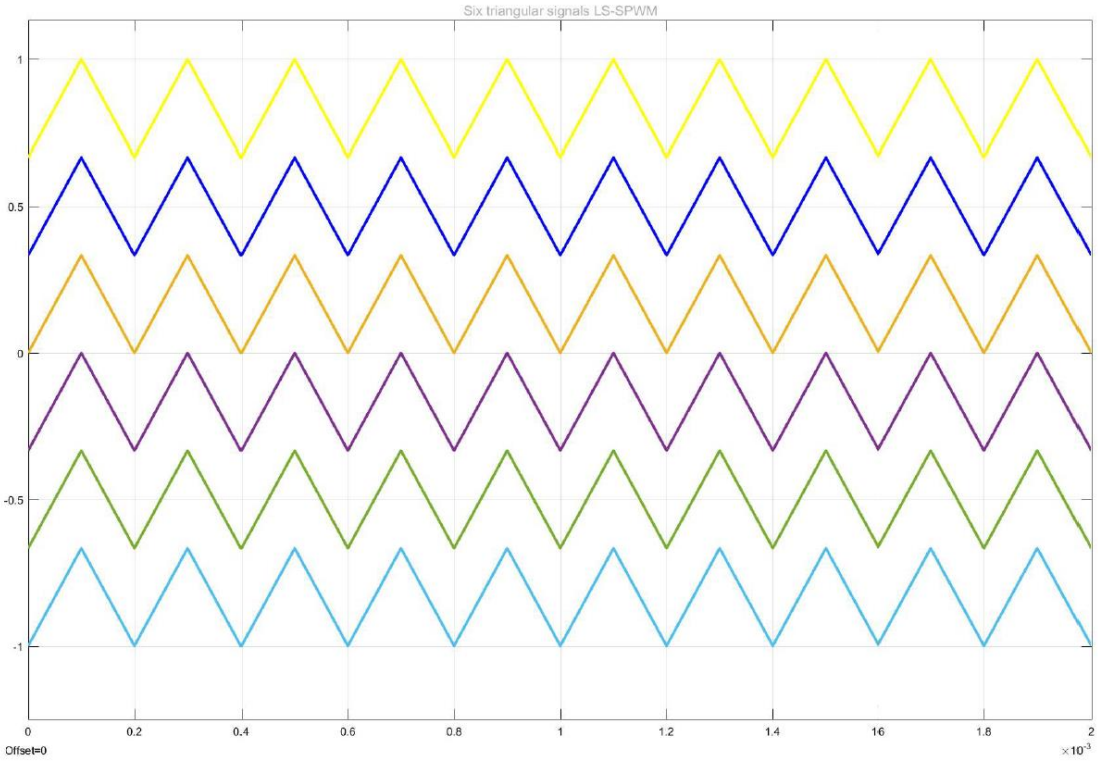


*Fig. 6-3 Six triangular LS-SPWM signals*

Whilst Figs. (6-4, 6-6) show the gate signals for phase-A switches in the 3 H-Bridges ($q_1$, $q_2$, $q_3$, $q_4$, $q_5$, and $q_6$), respectively. The reference signals for legs B, and C are the similar signals to that of leg A, but they are shifted 120° and 240°, respectively.

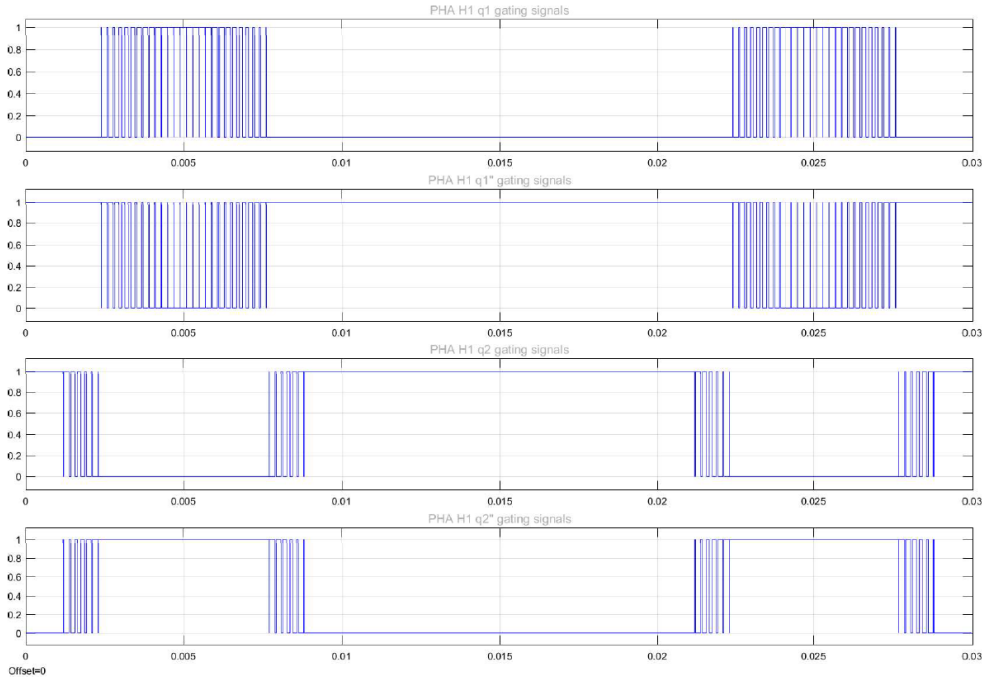


*Fig. 6-4 PHA HB1 gate signals*

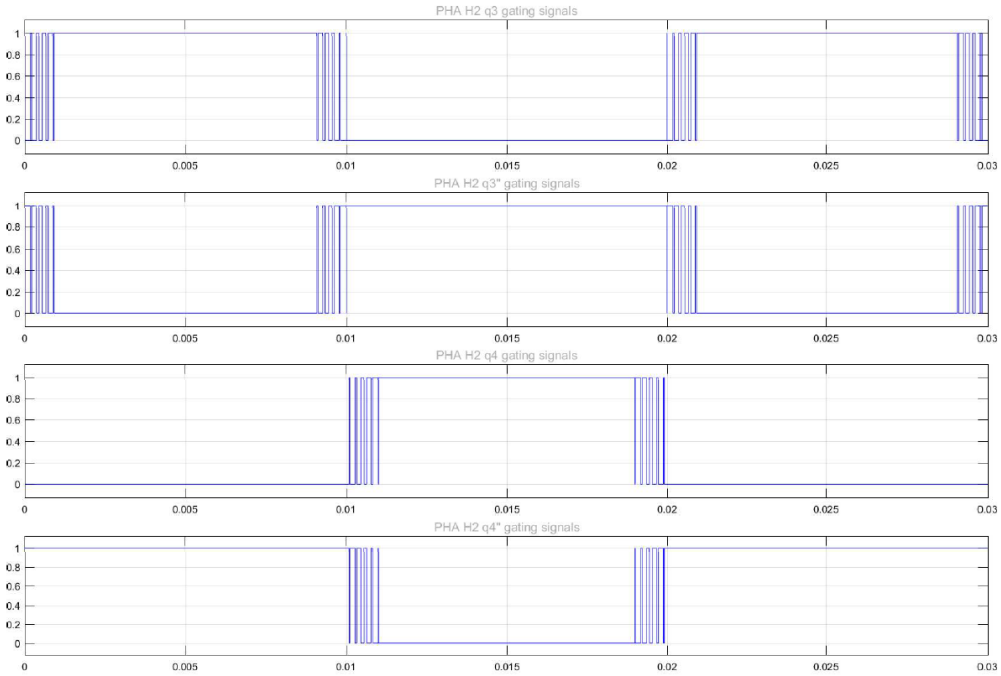


*Fig. 6-5 PHA HB2 gate signals*

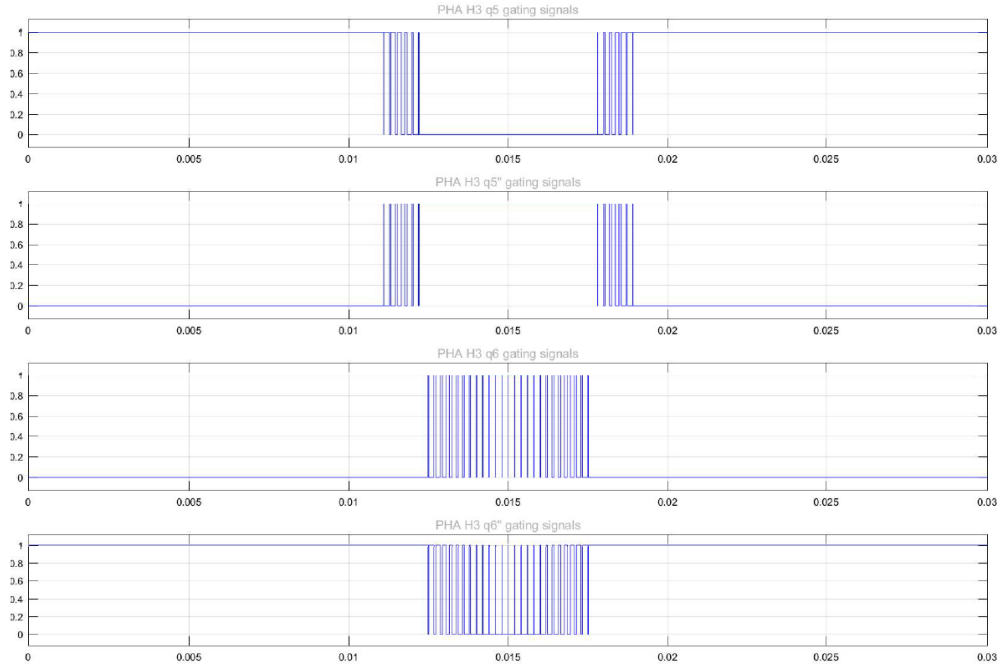


*Fig. 6-6 PHA HB3 gate signals*

Fig. 6-8 shows how gate signals for $H_1$ $q_1$ are generated via comparing the triangular signal with the carrier signal (a sinusoidal one).

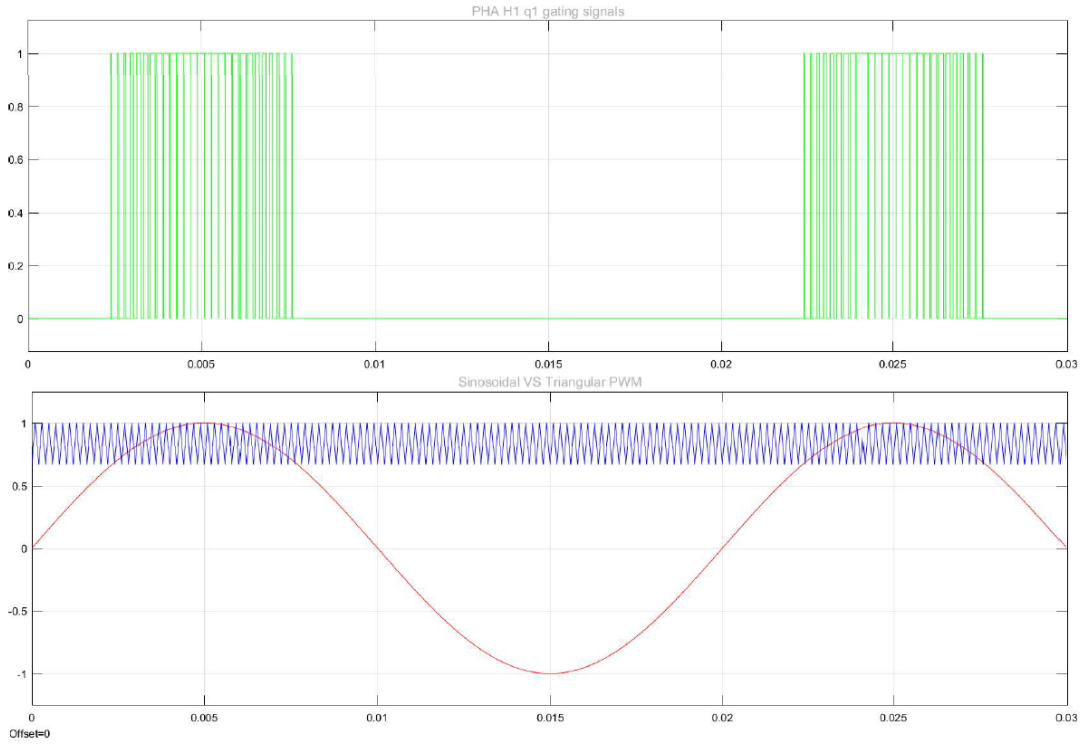


*Fig. 6-7 HB1 PHA q1 Sinusoidal VS Triangular PWM*

## 6.3 PV System Design

### 6.3.1 PV Array Design

The main purpose of the PV array in the design is to provide the DC-Link voltage as an input voltage for the inverter legs. In the THMLI, there are two types of the input voltage; the first one is $V_{dc}$, which is the input voltage for the first, $3V_{dc}$ for the second legs, and the $9*V_{dc}$ which is the input voltage of the third leg.

It is important to utilize the maximum power for all used PV arrays. But it is also important to have a regulated output voltage to serve the inverter input stage. The regulated output voltage will help to build a robust controller for the inverter. The controller manages the amount of injected active and reactive powers to the grid.

Basically, the PV stage of the system consists of four main sections:

1- PV array
2- Boost Controller
3- Filter
4- Controller

The PV array is designed to provide the input voltage of the Boost converter. In [58], $V_{dc}$ link value must be more than or equal to the twice of the rms value to the AC output voltage.

$$V_{dc} \geq 2V_m \tag{6.1}$$

Where, $V_m$ is the max value to the AC output voltage of the inverter phase. Thus, assuming that the grid's L-L voltage is $400V_{rms}$, $V_{dc}$ voltage will be:

$$V_{dc} \geq 2 * \sqrt{2}\frac{400}{\sqrt{3}} \geq 653V \tag{6.2}$$

In the inverter design, it is considered that the output voltage of the boost converter ($V_{dc}$ link voltage) to be 653V or more. Also, the reference $V_{dc}$ voltage of the controller (P-Q controller) to be 700V.

Ten strings consisting of 2 PV panels are used as a basic module for the first and the third legs of the inverter. And, 10 strings of 6 PV panels are used as a basic module for the second leg. Table 6-1 shows the information about the used PV panel/arrays for each leg.

*Table 6-1 PV array design parameters*

| No. | PV Panel Type | Inverter Leg | Parallel | Series | Voc | Vin | Isc | Power [W] |
|---|---|---|---|---|---|---|---|---|
| **1** | Jinko Solar JKM310M-72 | 1 | 8 | 1 | 38.5 | 38.5 | 8.78 | 2480 |
| **2** | Jinko Solar JKM310M-72 | 2 | 8 | 3 | 38.5 | 115.5 | 8.78 | 7440 |
| **3** | Jinko Solar JKM310M-72 | 3 | 8 | 9 | 38.5 | 346.5 | 8.78 | 22320 |
| | | Total Power [W] | | | | | | 32240 |

Concerning the environmental conditions, two options were considered. The first option is the standard conditions of irradiation 1000W/m$^2$ and temperature 25$^\circ$ . And the selected various conditions of irradiation and temperature to figure out the behavior of the inverter under these conditions. Fig. 6-8 shows both options and Fig. 6-9 shows the various environmental input conditions of the PV arrays.

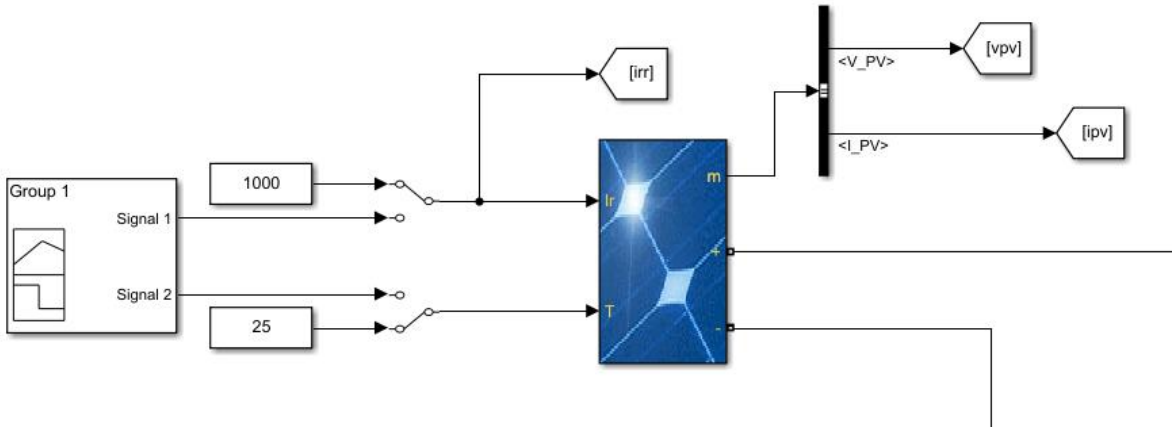


*Fig. 6-8 PV Array model*

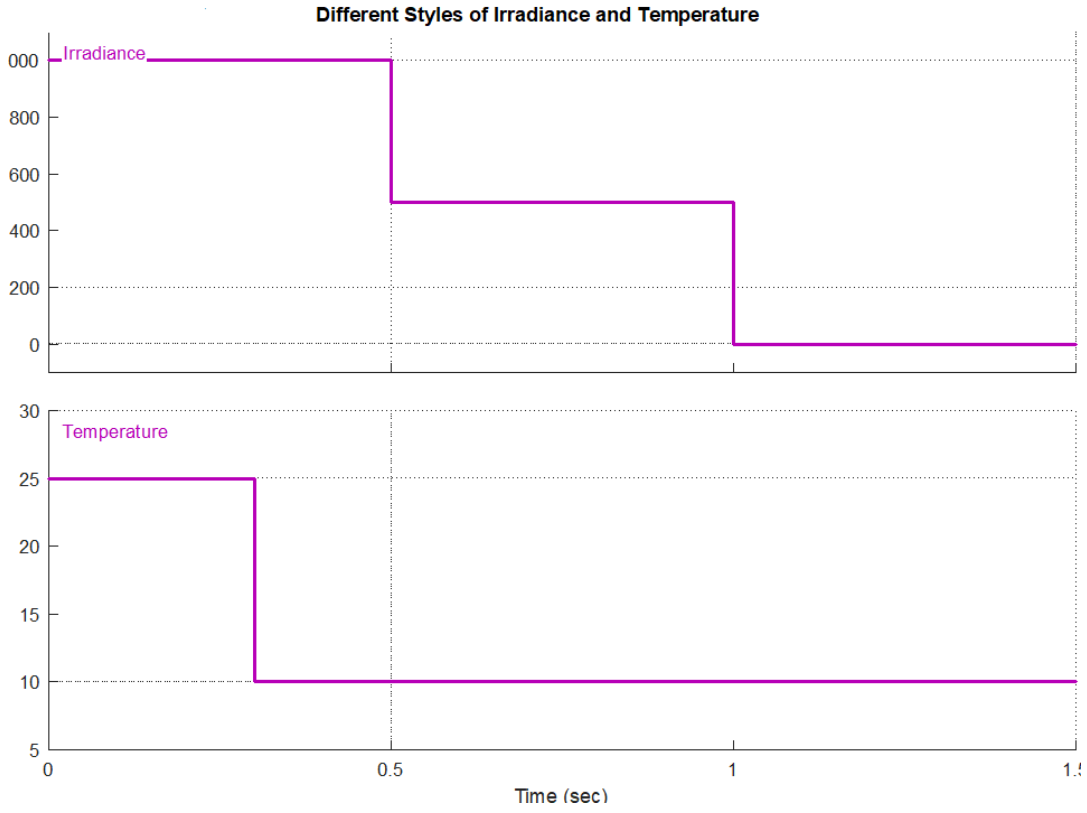


*Fig. 6-9 Environmental Conditions - Various Irradiation and Temperature*

### 6.3.2 Boost Converter Design

There are two main goals of using the Boost converter in the PV HMLI design:

1- Raise the PV input voltage to the required voltage value of the inverter DC-Link input.
2- Get a regulated output in various environmental conditional and various loads.

Fig. 8-10 shows the used design of the Boost converter.

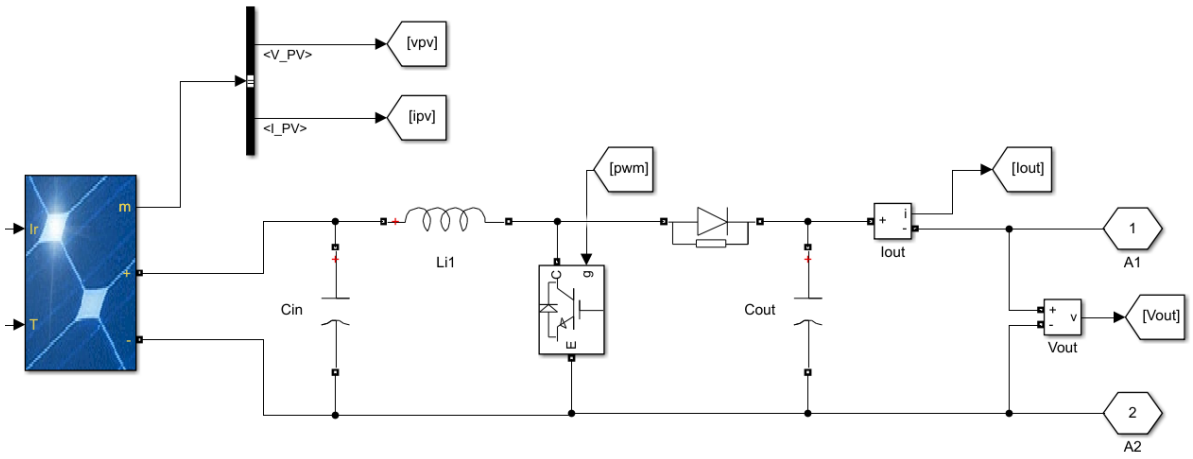


*Fig. 6-6-10 Boost Converter*

The value of the output voltage, the mode of operation, and the voltage ripple determine the design parameter values of the converter. The input capacitor is necessary to stabilize the output voltage of the PV array due to the peak current requirement of the PV voltage. The value of the capacitor can be increased if the PV voltage is noisy [74]. The capacitor's value in the inverter design is given in eq. (6.3) [75]

$$C_{pv} = \frac{V_{pv}}{2\pi f \Delta v_{pv} R_{pv}} = \frac{38.5}{2 * 3.14 * 50 * 2 * 8} = 0.0075F \tag{6.3}$$

where $V_{pv}$, $\Delta v_{pv}$, $R_{pv}$ and $f$ are the DC voltage of the PV array, the voltage ripple, the DC output resistance of the PV array and the frequency, respectively.

Since it is an on-grid inverter and duty ratio of the boost converter is always changing depending on the various operating conditions of the inverter, the design will be selected based on the worse conditions. Supposing that the efficiency of the design is 90%, eq. 6.4 shows the calculation of the duty ratio.

$$D = 1 - \frac{V_{in} * \eta}{V_{out}} = \frac{38.5 * 0.9}{54} = 0.6 \tag{6.4}$$

where, $V_{in}$ is the output voltage of the PV array and $V_{out}$ is the output voltage of the boost converter. The output voltage of the boost converter for the first leg of the inverter is determined by eq. (6.5):

$$V_{out} = \frac{V_{dc-link}}{\#\ of\ basic\ modules} = \frac{700}{13} = 54V \tag{6.5}$$

The value of the inductor determines the mode of the operation. There are three types of operation in which the boost converter can operate:

- $L_i < L_{crit}$ : Discontinuous Conduction Mode (DCM)
- $L_i = L_{crit}$: Boundary Conduction Mode (BCM)
- $L_i > L_{crit}$: Continuous Conduction Mode (CCM)

The critical value of the inductor is given by eq. (8.6):

$$L_{crit} = \frac{V_{in}^2 DT}{2 * V_{out}} \tag{6.6}$$

Depending on the value in Table 6-1, the critical value of the inductor is 0.3813mH. It is proposed to operate the converter in the continuous mode. And so, the inductor's value used in the design is 10 times the critical value; 3.813mH.

On the other side the ripple percentage of the output voltage determines the value of the capacitor. In order to get the best steady voltage at the output that can easily work with the Level-Shift SPMW controller, the voltage ripple is assumed to be 1% of the output voltage. Equation 6.7 shows the calculation of the capacitor's value depending on the provided parameters and considering a minimum value of R_load; $R = 5\Omega$. With $V_{out} = 54$, $D = 0.6$, $T = 2.56\mu s$, $\Delta V_{out} = 0.01$, and $R = 5$, the capacitor's value can be calculated as:

$$C = \frac{V_{out} * DT}{\Delta V_{out} * R} = 0.01F \tag{6.7}$$

## 6.4 Coupling LCL Filter Design

In [71] and [76] , the design procedure of the LCL filter depends basically three parameters; the rated power of the inverter, the grid's frequency, and the switching frequency. Based on the per-unit calculations, the filter parameters depend on eqs. (6.8) and (6.9):

$$Z_b = \frac{V_{Ln}^2}{P_n} \tag{6.8}$$

$$C_b = \frac{1}{\omega_n Z_b} \tag{6.9}$$

Where, $Z_b$ is the base impedance, $V_{Ln}$ is the Line-to-Line rms voltage, $P_n$ is the rated power of the inverter, and $\omega_n$ is the rated frequency of the grid. The resonance frequency ($\omega_{res}$) is related to the switching frequency ($\omega_{sw}$) using eq. (6.10). It must be between 10 times of the grid frequency and one-half of the switching frequency [76];

$$\omega_{res} = k\omega_{sw} \tag{6.10}$$

Where, k is a factor of how far the resonance frequency is from the switching frequency.

In the grid's filter design, there are some constraints, which limit the value of the filter parameters and have to be taken into consideration:

1- The filter capacitance is selected according to the decrease of the power factor ($pf$) at the rated power at the Point of the Common Coupling (PCC). Generally, this limit is less than 5% [76]. Therefore, the filter capacitor value can be determined as illustrated in eq. (6.11):

$$C_f = xC_b = \frac{x}{\omega_n Z_b} = \frac{x}{2\pi f_n Z_b} \tag{6.11.a}$$

$$C_f = \frac{P_n}{2\pi f_n V_{Ln}^2} = 30.8\mu F \tag{6.11.b}$$

2- The inductor of the invertor side ($L_i$) is determined following the current ripple as a criterion. The value of the inverter side inductor depends on the DC voltage, the switching frequency and the amplitude modulation index. Equation (6.12) shows how the maximum ripple of the output current can be calculated [71]:

$$\Delta I_{l,max} = \frac{2V_{dc}}{3L_i f_{sw}}\, m(m-1) \tag{6.12.a}$$

$$L_i = \frac{2V_{dc}}{3\Delta I_{l,max} f_{sw}}\, m(m-1) \tag{6.12.b}$$

As the amplitude modulation index value varies between 0 and 1, the maximum value of the current ripple will occur at m=0.5 [71].

$$\Delta I_{l,max} = \frac{V_{dc}}{6 L_i f_{sw}} \tag{6.12.c}$$

$$L_i = \frac{V_{dc}}{6 \Delta I_{l,max} f_{sw}} \tag{8.12.d}$$

As a common practice, the value of the current ripple equals 5-25% of the maximum output current (here considered as 5%). Equation (6.13) shows the calculation of the maximum current[61],[66],[68]:

$$I_{l,max} = \frac{\sqrt{2} P_n}{3 V_{ph}} \tag{6.13.a}$$

$$\Delta I_{l,max} = 0.05 \frac{\sqrt{2} P_n}{3 V_{ph}} \tag{6.13.b}$$

Where, $V_{ph}$ is the phase voltage. Thus, eq. (6.14) shows the final calculation of the inverter side inductor.

$$L_i = \frac{10 V_{dc} V_{ph}}{\sqrt{2}\, P_n f_{sw}} \tag{6.14}$$

3- The accumulative value of the inductance should be less than 0.1 pu ($L_b = \frac{Z_b}{\omega_n}$) to limit the value of the AC voltage drop during the operation of the inverter [62].
4- The value of the grid side inductor can be also calculated depending on the ripple current criterion [62], [71], and [74]. This is shown by eq. (6.15):

$$K_a = \frac{1}{\left|1 + r\left[1 - L_i C_f \omega_{sw}^2\right]\right|} \tag{6.15}$$

Where, $K_a$ is the harmonic attenuation factor (assumed 20%) at the switching frequency, and r is the ratio factor between the grid and inverter inductors ($r = {L_g}/{L_i}$).

5- To avoid the resonance occurrence, a damping resistor is connected in series with the filter capacitor, $C_f$. Equation (6.16) shows how the damping resistance is calculated [61], [62], and [71]:

$$R_d = \frac{1}{3\, C_f \omega_{sw}} \tag{6.16}$$

## 6.5 Active and Reactive Power Controllers

Traditional control methods that are usually used in the symmetrical inverters are effective to be used in the asymmetrical MLIs [77]. Depending on the reference frame transformation techniques, a decoupled control scheme cab be developed for controlling the active and reactive powers produces by the HMLIs.

### 6.5.1 3-phase to the Stationary Reference Frame Transformation (Clarke Transformation) ($\boldsymbol{abc \rightarrow \alpha\beta}$)

Both 3-phase voltages and current are time varying variables according to the dynamics of each individual phase. Therefore, the mathematical model of three phase system is complicated. In order to facilitate the calculation of the three phase parameters, they can be represented in the stationary reference frame as two phases, as shown by eq. (6.17):

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{6.17}$$

### 6.5.2 Stationary Reference Frame to the Synchronous Reference Frame Transformation (Park Transformation) ($\boldsymbol{\alpha\beta \rightarrow dq}$)

Although the Clarke Transformation converts the 3-phase variables into two variables, the Stationary Reference variables still rotating at the same speed of the original three phase AC variables. That matter affects the control design and complicates the tracking process of the $\alpha\beta$ variables. The Park Transformation converts the stationary rotating variables into a synchronous reference frame variables as shown in eq. (6.18).

$$\begin{bmatrix} x_d \\ x_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \tag{6.18}$$

### 6.5.3 Current Control Loop

The aim of this control loop is to regulate the output current of the inverter by generating a proper output voltage reference. For simplicity, if the output coupling filter is an LC filter, the output relationship between the voltage and the current is represented by eq. (6.19):

$$L\frac{di}{dt} + Ri = v_1 - v \tag{6.19}$$

Where, $i$ $v_1$, and $v$ are the output current, the output voltage and the load voltage, respectively. And R is the internal resistance of the inductor, and L is the accumulative inductance of the filter and the grid.

Applying both Clarke and Park frame transformation to eq. (6.19), results in the synchronous reference frame shown in eq. (6.20):

$$\begin{aligned} L\frac{di_d}{dt} + Ri_d - \omega L i_q &= v_{d1} - v_d \\ L\frac{di_q}{dt} + Ri_q + \omega L i_d &= v_{q1} - v_q \end{aligned} \tag{6.20}$$

where $i_d, v_{q1}, v_q$,…. are ….L and R ….

Both perpendiqular components of the synchronous frame $i_d$ and $i_q$ can be controlled by regulating the corresponding output voltages $v_{d1}$ and $v_{q1}$. By doing some modifications to eq. (6.20) keeping each current component in the left side, the output reference voltages will be generated as illustrated in eq. (6.21):

$$\begin{aligned} v_{d1}^* &= v_{d1} + \omega L i_q - v_d \\ v_{q1}^* &= v_{q1} - \omega L i_d - v_q \end{aligned} \tag{6.21}$$

Finally, eq. (6.22) is the characteristic equation that represents the current control loop:

$$\begin{aligned} L\frac{di_d}{dt} + Ri_d &= v_{d1}^* \\ L\frac{di_q}{dt} + Ri_q &= v_{q1}^* \end{aligned} \tag{6.22}$$

### 6.5.4 P-Q Control Loop

In the synchronous DQ reference frame, the instantaneous active power, P, and reactive power, Q, are given by equation 6.23 [58] and [77]:

$$\begin{aligned} \mathrm{P} &= \frac{3}{2}\left(v_d i_d + v_q i_q\right) \\ \mathrm{Q} &= \frac{3}{2}\left(v_q i_d - v_d i_q\right) \end{aligned} \tag{6.23}$$

Taking into consideration that a Phase Locked Loop (PLL) is aligned with the load voltage vector to the d-axis of the dq reference frame, the transfer functions will be as shown in eq. (6.24) [77]:

$$\begin{aligned} \frac{P(s)}{i_d(s)} &= \frac{3}{2} v_d(s) = \frac{3}{2} V_m \\ \frac{Q(s)}{i_q(s)} &= -\frac{3}{2} v_d(s) = -\frac{3}{2} V_m \end{aligned} \tag{6.24}$$

### 6.5.5 DC-Link Control Loop

This loop is usually used instead of the active power control loop in the PV inverters to maintain the DC-link voltage constant. That ensures all the extracted power from the PV arrays can be totally delivered to the AC load. According to power conservation, the ouptut AC power of the inverter equals the input DC power as shown by eq. (6.25) [77]:

$$v_{dc} C_{dc} \frac{dv_{dc}}{dt} = \frac{3}{2}\left(v_d i_d + v_q i_q\right) \tag{6.25}$$

where $C_{dc}$ is ….

Taking into consideration that, the PLL is aligned with the load voltage vector to the d-axis of the dq reference frame, the transfer function will be as shown in eq. (6.26):

$$\frac{v_{dc(s)}}{i_d(s)} = \frac{3}{2} \frac{V_m}{V_{dc} C_{dc} s} \tag{6.26}$$

# Chapter 7. MATLAB/Simulink Simulation

## 7.1 HMLI MATLAB/Simulink Simulation

In MATLAB/Simulink model for the HMLI, the following topologies and parameters were used:

- Three-phase inverter
- 3 H-bridge modules are used for each phase
- The switching frequency equals 5,000Hz
- Level-shift SPWM
- Bipolar switching pattern
- Ideal IGBTs switches

## 7.2 MATLAB/Simulink Model Parts

Fig. 7-1 shows the whole Matlab/Simulink schematic of the HMLI, whilst Fig. 7-2 shows the method of generating the gate signals for the IGBTs depending on the level-shift sinusoidal pulse width modulation. It basically generates 6 triangular signals to be compared to a fundamental sinusoidal signal, that is generated depending on the Vdc-link and P-Q controllers following the bipolar switching pattern, and the carrier frequency equals 50Hz, whereas the switching frequency equals 5,000Hz. For each phase of the inverter, three H-bridges were used with different isolated PV arrays (that's why the inverter is already named hybrid) $V_{dc1} = 54V$, $V_{dc2} = 162V$ and $V_{dc3} = 486V$. Besides, the sinusoidal (modulating) signals for the three phases are shifted by $120^{\circ}$.

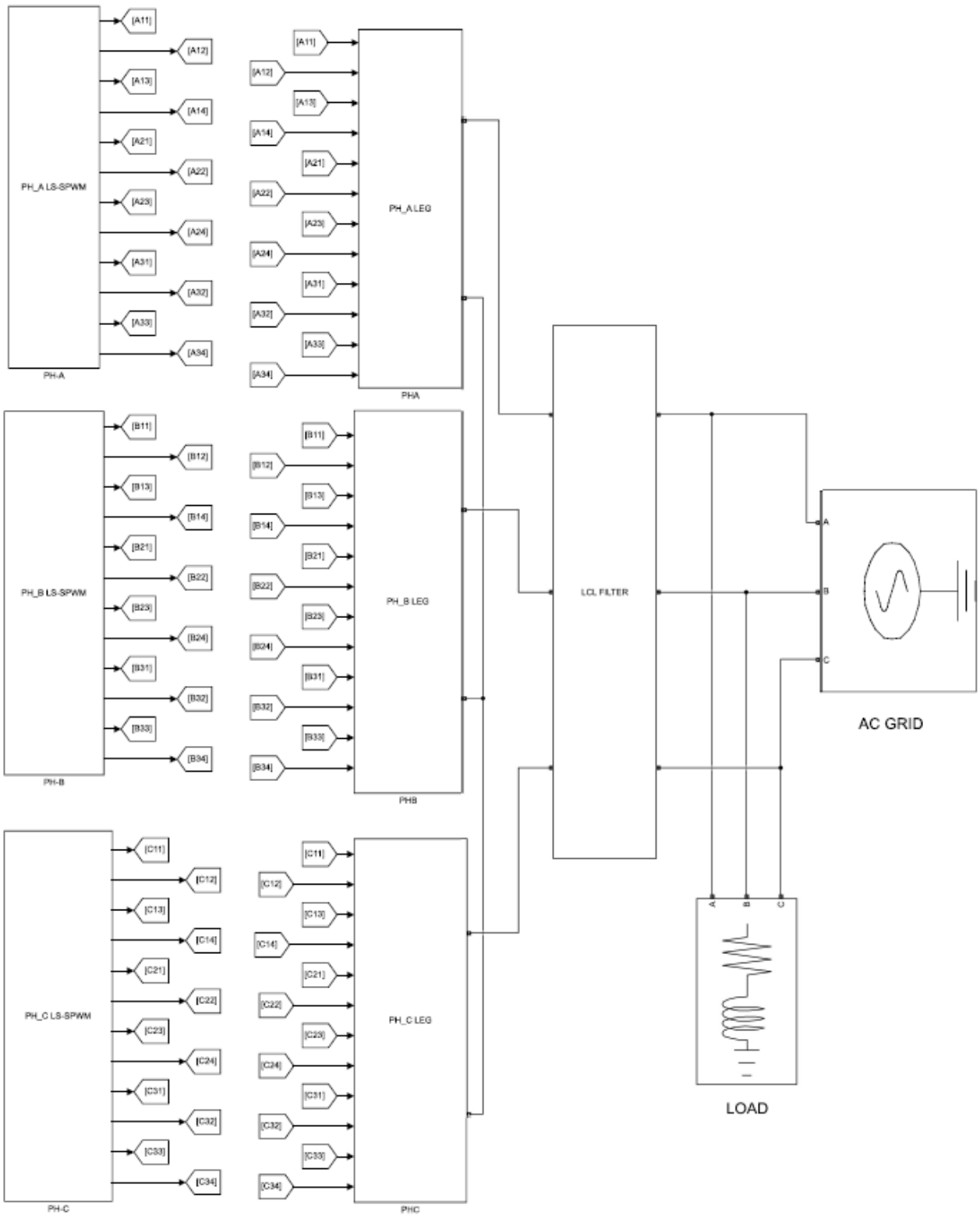


*Fig. 7-1 General Overview of the HMLI*

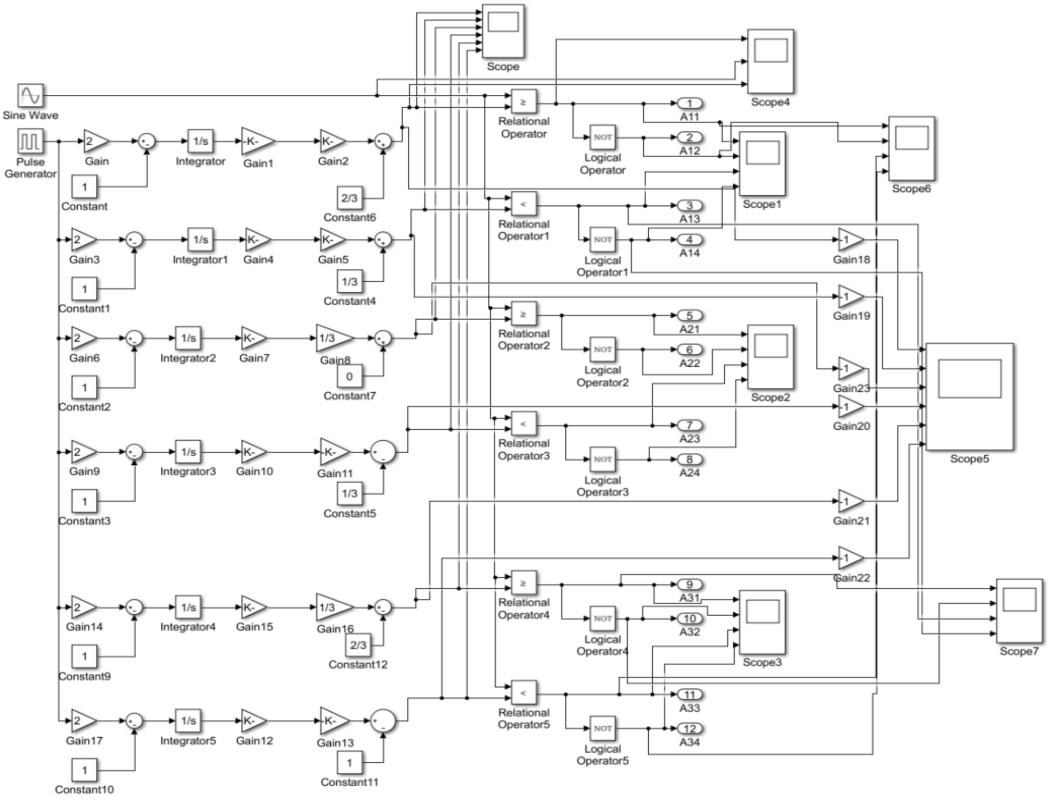


*Fig. 7-2 THMLI Level-Shift Pulse Width Modulation Generation Blocks*

The schematic of the single-phase leg of the inverter is shown in Fig. 7-3. As mentioned previously, ideal switches are used, and so there is no need for the deadtime between the gate signals of the two switches in each leg ($q_n$ *and* $q_n'$ ).

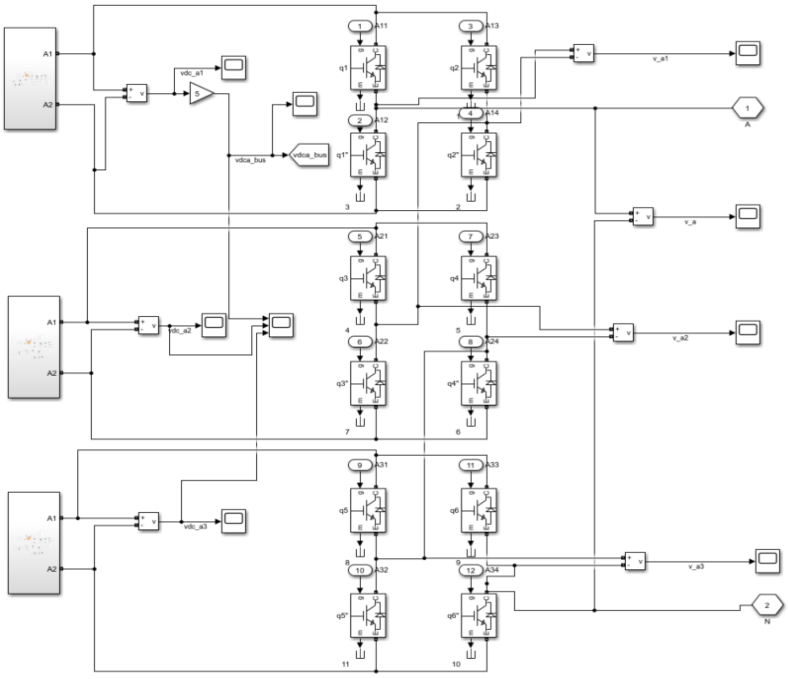

*Fig. 7-3 $Phase_A$ Schematic Structure*

Fig. 7-4 shows the PV array with different environmental conditions. The PV array design includes the controller of the Boost converter. The controller is designed to produce a regulated output voltage. That helps constructing a robust and reliable P-Q controller in the advanced stage of the whole system.

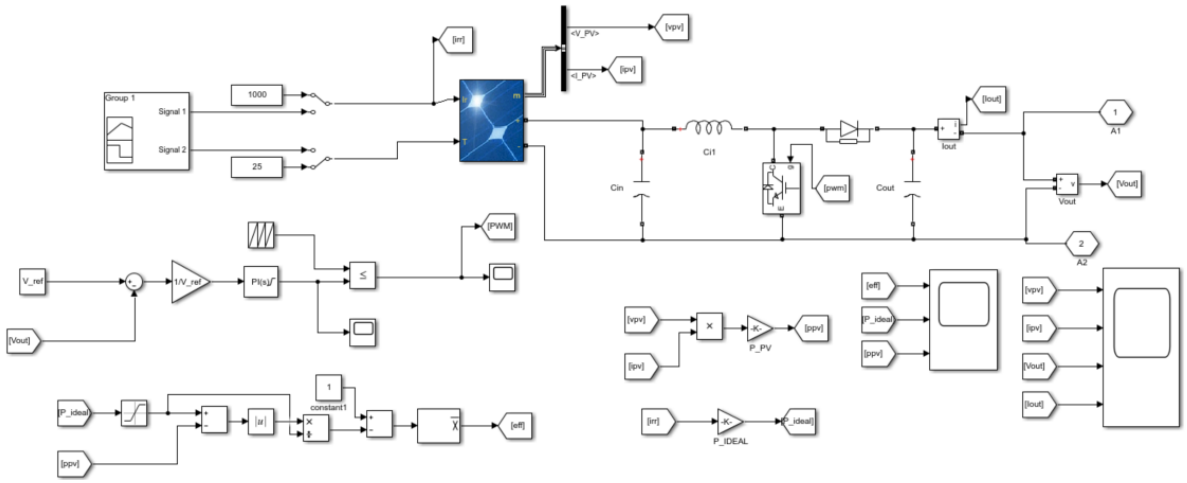

*Fig. 7-4 PV Array Design*

The Boost converter is shown in Fig. 7-5. The PV array provides the input voltage for the boost converter. The switch of the converter is controlled using PWM gate signals generated by the controller shown is Fig. 7-6. This schematic is used in the three legs for the three phases in the inverter. Each boost converter has the design parameters depending on the specific input voltage and the required output voltage.

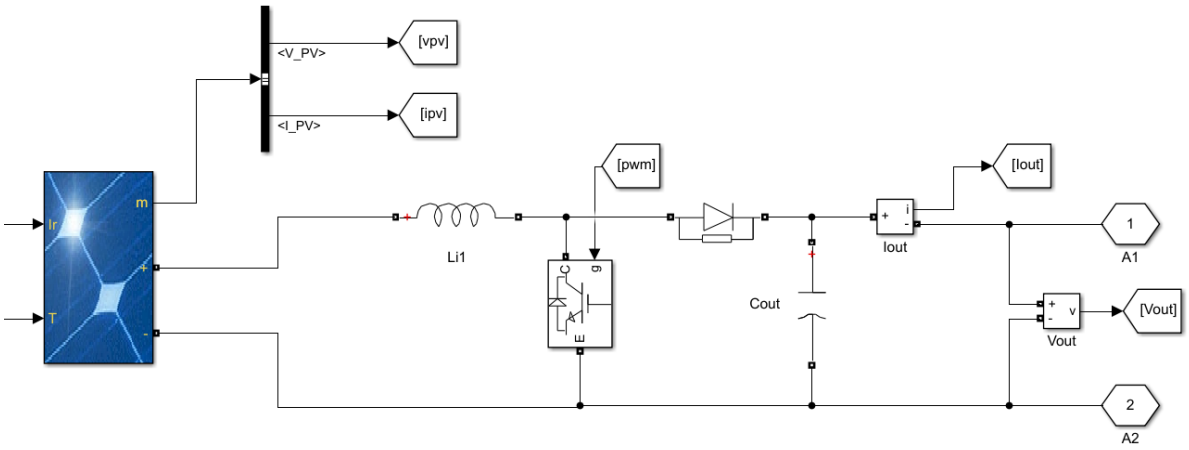


*Fig. 7-5 Boost Converter Model*

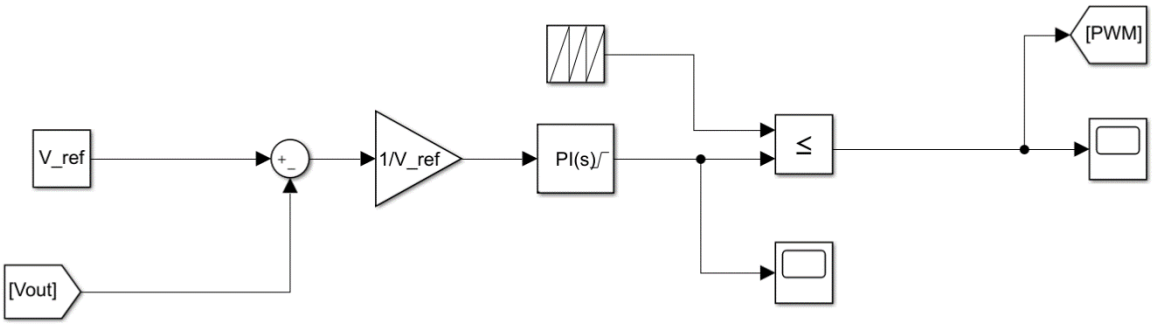


*Fig. 7-6 Boost Converter Controller*

The LCL filter schematic and how it is connected between the inverter and the grid is shown in Fig. 7-7. A very low value resistance is added to the inductors as a self-internal resistance in both inverter and grid sides (1% of the inductor's value). The grid is 400V ph-ph and 50Hz power supply. Voltage and current measurements are added in both sides, in order to monitor and compare signals at the coupling point, and to generate the required control signals for P-Q controllers.

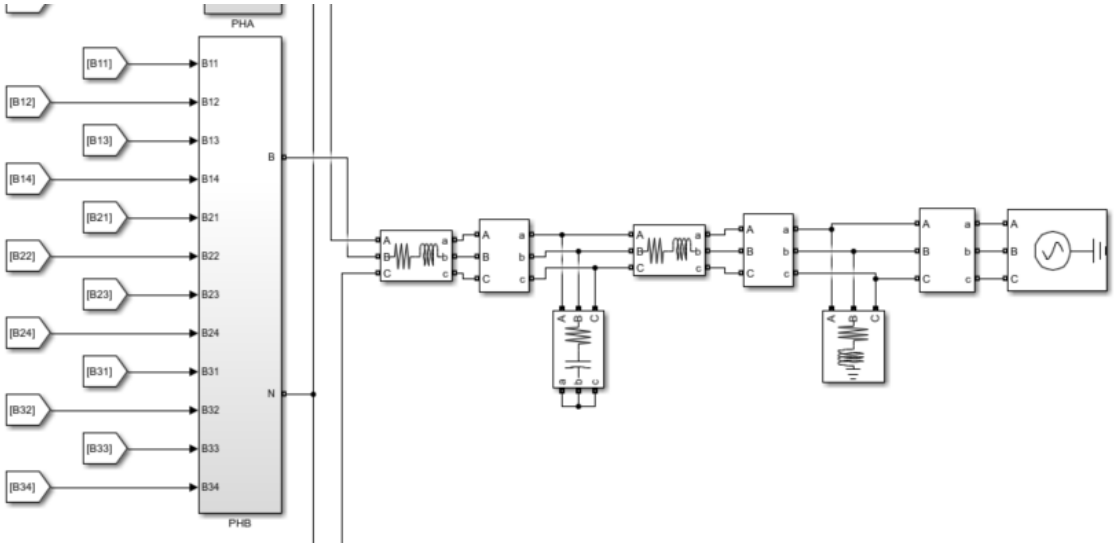


*Fig. 7-7 LCL Filter Connection*

Figs. 7-8 and 7-9 show the generation block of both grid and inverter $dq$ voltages, currents, active and reactive powers, respectively.

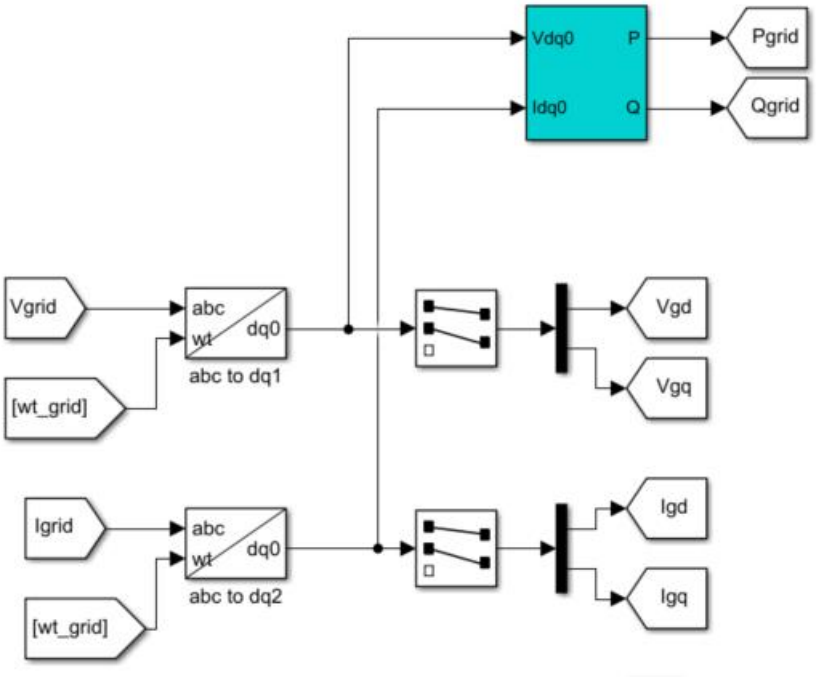


*Fig. 7-8 Grid abc to dq Conversion*

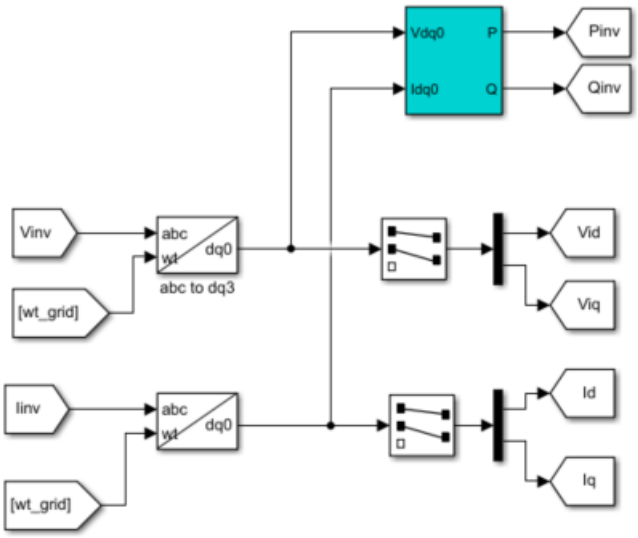


*Fig. 7-9 Inverter abc to dq Conversion*

Fig. 7-10 shows the controllers of the $V_{dc}$, active, and reactive powers. Meanwhile, Fig. 7-11 shows the inside details of the controllers. The generation of the reference signal is shown in Fig. 7-12.

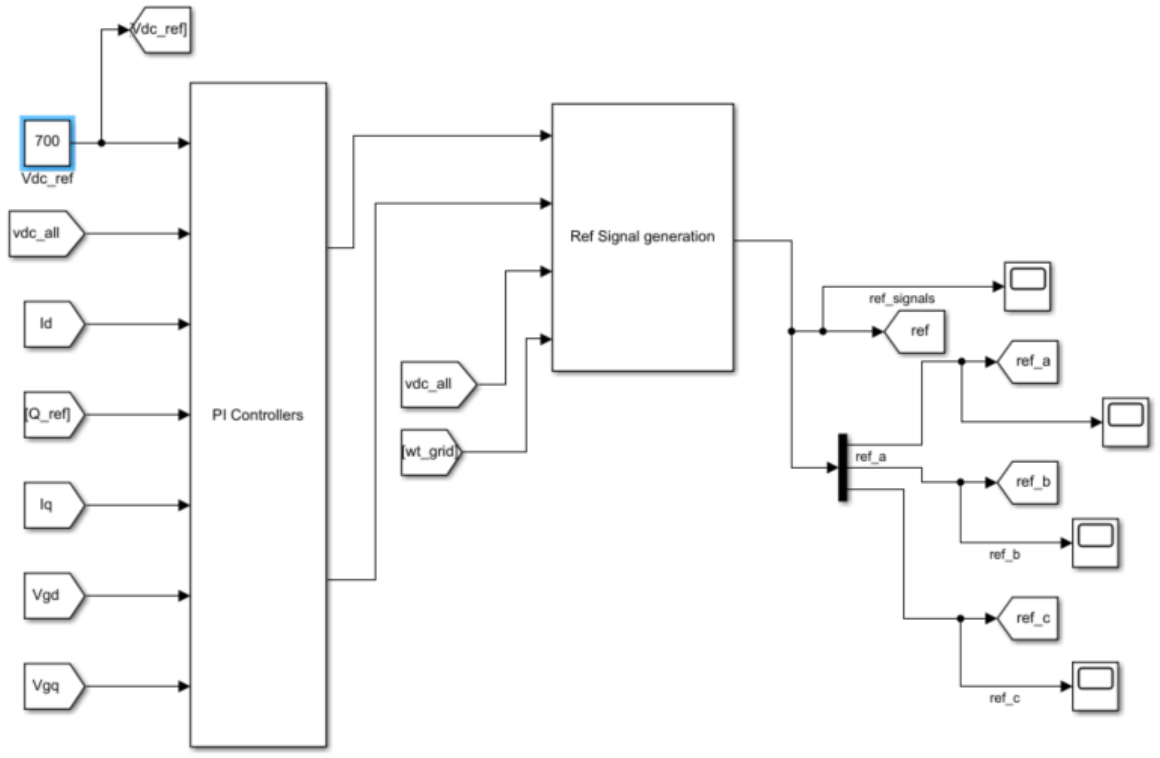


*Fig. 7-7-10 Vdc, P, and Q Controllers*

The controller receives 7 control signals. $V_{gd}$ and $V_{gq}$, and $wt$_grid are generated from the grid side to control to the output voltage of the converter. The output voltage of the inverter has to be almost the same of the grid's voltage (Shape, frequency, phase shift, and the amplitude). Id and Iq are the decoupled output current components of the inverter. They are used to control the power injected into the grid based on the reference values P_ref and Q_ref. Also, Vdc_ref is added to control the outer control loop that connects the output of the inverter with the DC-link input voltage (controlled also by the boost converter).

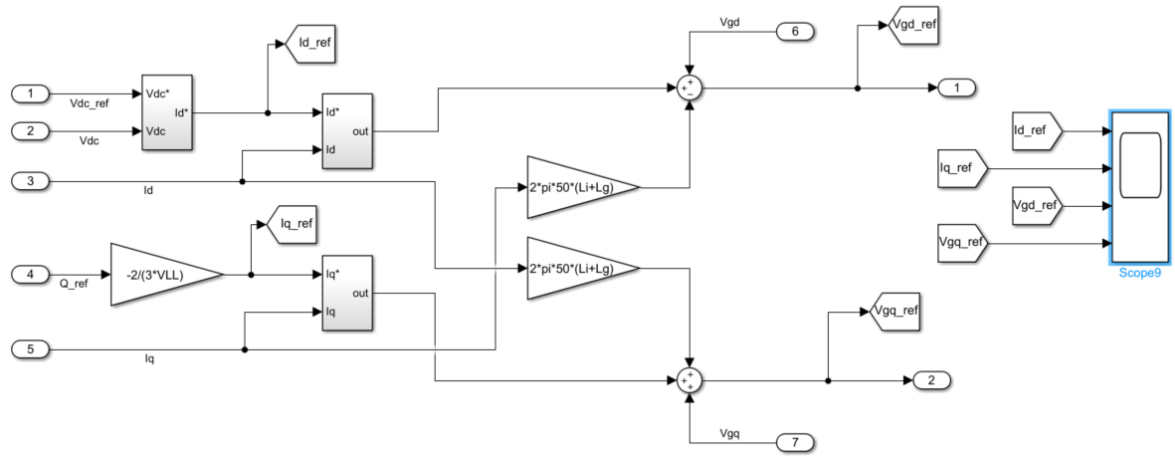


*Fig. 7-11 Id_ref, Iq_ref, Vd_ref and Vq_ref Controllers*

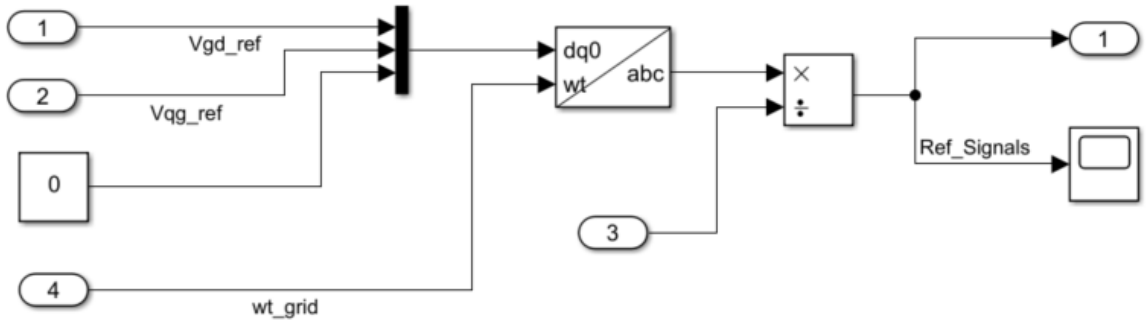


*Fig. 7-12 Reference Signals Generation*

Fig. 7-13 shows the six triangular signals used to generate the gate signals for the switches. Those six signals are the basic ones used for the first phase of the inverter (Ph-A). These signals are shifted by $120^{\circ}$ and $240^{\circ}$ to be used for the remaining phases of the inverter (Ph-B) and (Ph-C), respectively.

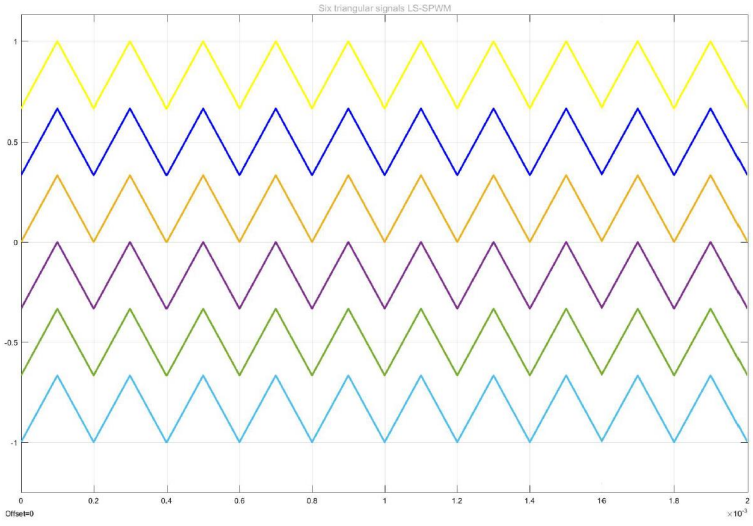

*Fig. 7-13 Six triangular LS-SPWM signals*

## 7.3 Matlab Results and Analysis

In order to demonstrate all possible conditions that the inverter may operate under, this section is divided into four sub-sections. The first section is to demonstrate the various conditions applied to the all three inputs of the inverter equally, the second one is to demonstrate the conditions applied on one phase only, the third is to demonstrate the conditions applied on two phases, and the last one is to demonstrate the effect of changing the reference active and reactive powers.

### 7.3.1 General Conditions – Simulation and Results

Keeping the load constant and injecting the same reference values of the active and reactive powers to the grid, various environmental conditions are applied to all the PV arrays of the inverter. The value of the irradiation, and the value of the temperature are shown in Fig. 7-9. The active power reference is the full capacity of the inverter which is 31kW and the reactive power reference value is 5% of the full capacity.

Fig. 7-14 shows the input and output voltages and currents of the PV array in the second leg of the inverter. It is shown that, the voltage of the PV array and the output voltage are affected slightly by the decreasing of the ambient temperature degree. Also, the voltages are proportionally affected by changing the irradiation rate. However, there is no significant effect on the output current of the boost converter.

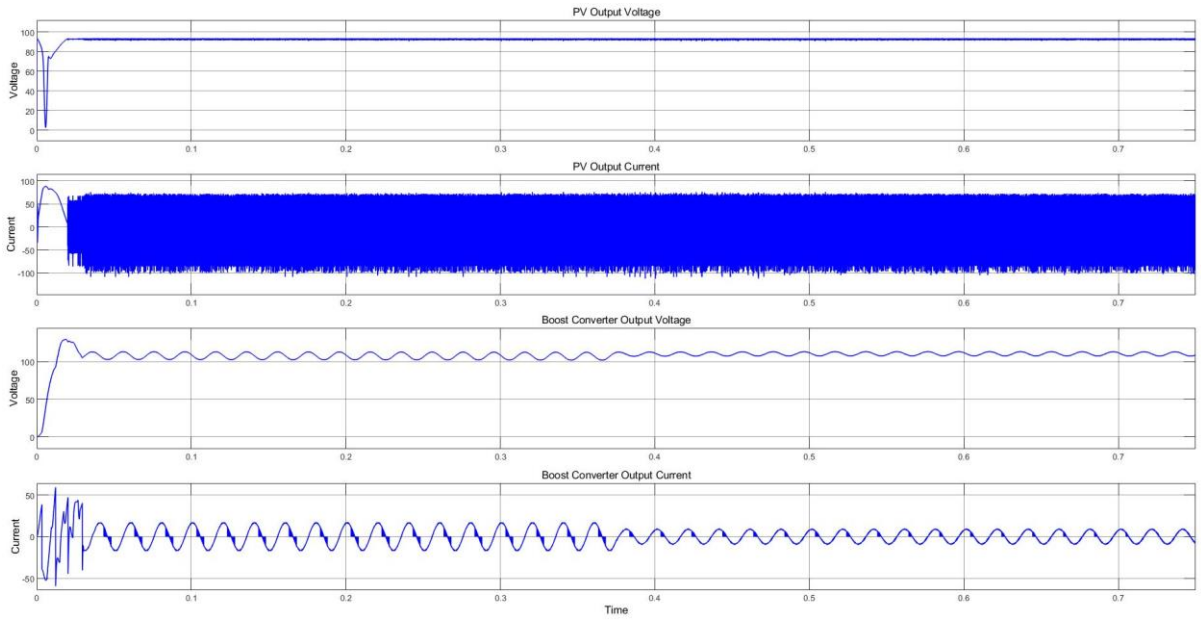


*Fig. 7-14 Input and Output Voltages and Currents of the PV array - 2nd Leg of the Inverter*

Figs. 7-15 and 7-16 show the number of levels in the L-N and L-L voltages, respectively. There are 7 levels in the L-N voltages, and 15 levels in the L-L voltages.

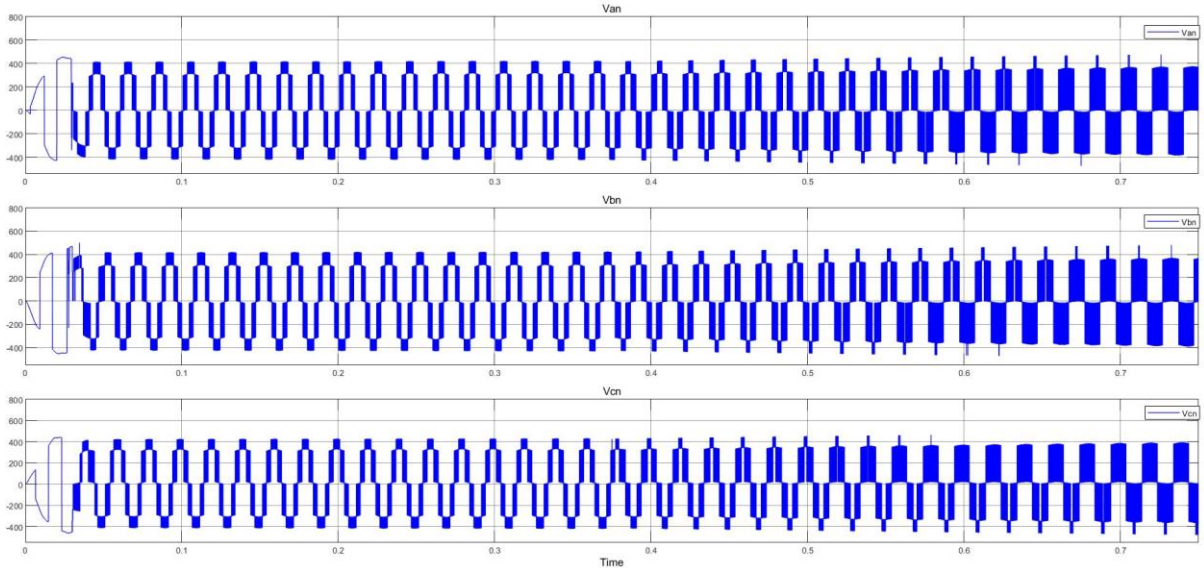


*Fig. 7-15 L-N Voltage Levels*

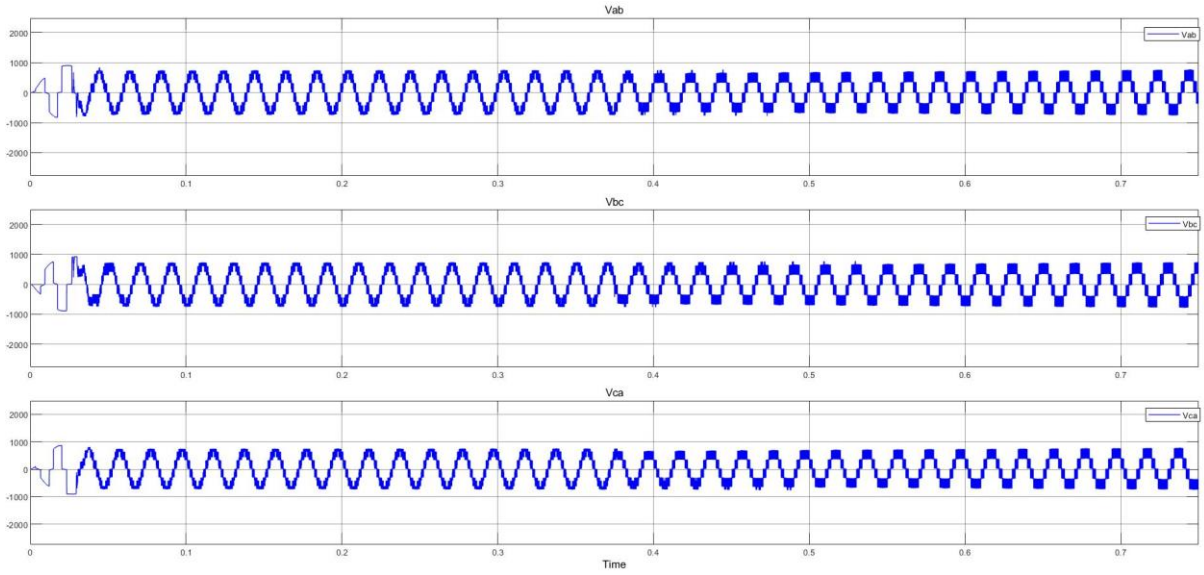


*Fig. 7-16 L-L Voltage Levels*

According to the total harmonic distortion, Fig. 7-17 shows the Fast Fourier Transform for line-to-line voltage $V_{AB}$ before the filter, which shows that the value of THD equals 0.24%.

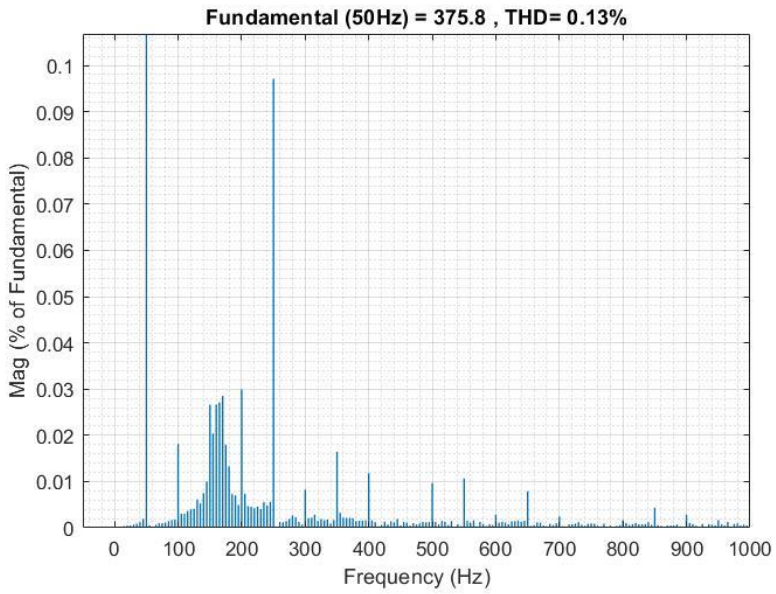


*Fig. 7-17 Fast Fourier Transform for V_(L-L)*

Concerning to the output current of the inverter, Fig. 7-18 shows the effect of the environmental factors on the output current before the filter. In addition, Fig. 7-19 shows the effect on the output current after the filter. Besides, Fig. 7-20 shows the effect on the output voltage of the inverter.

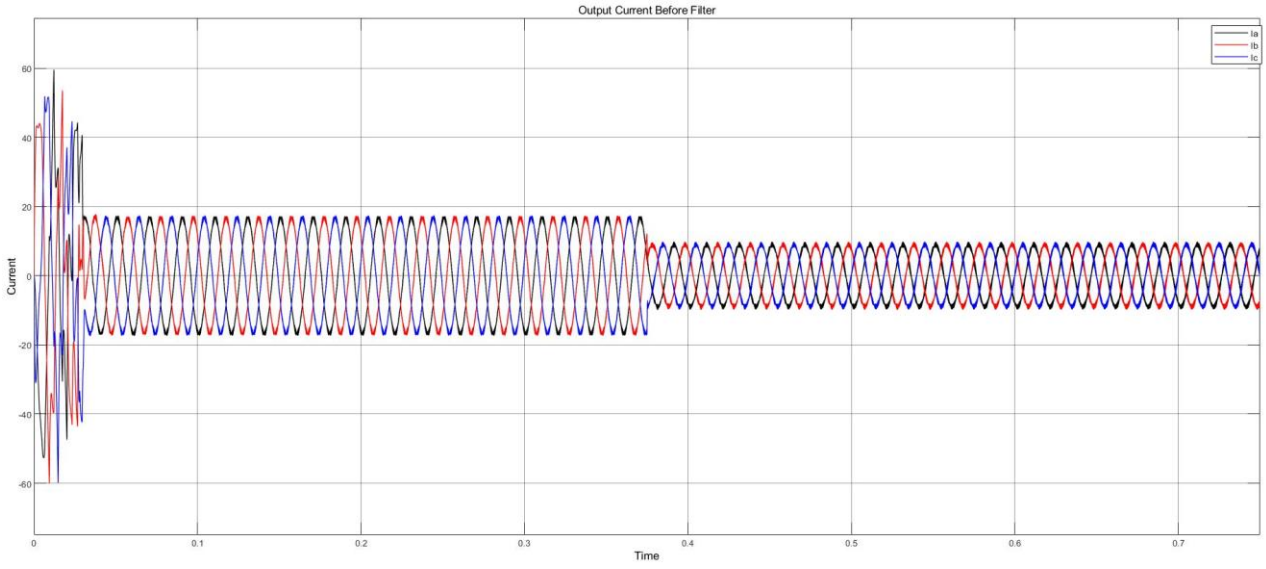


*Fig. 7-18 Inverter Current before the Filter*

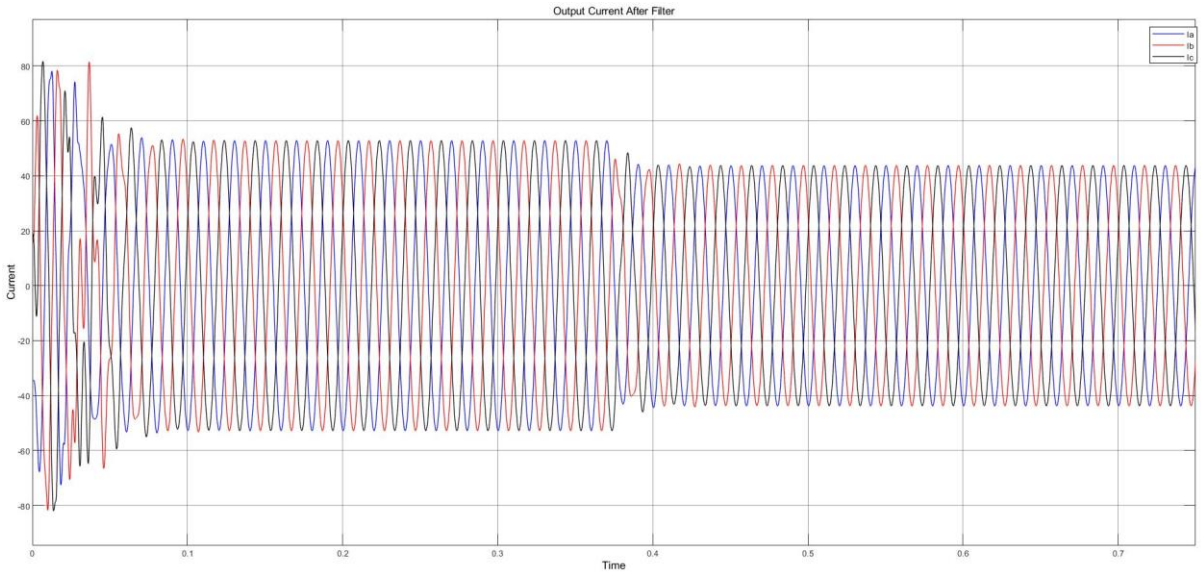


*Fig. 7-19 Inverter Current after the Filter*

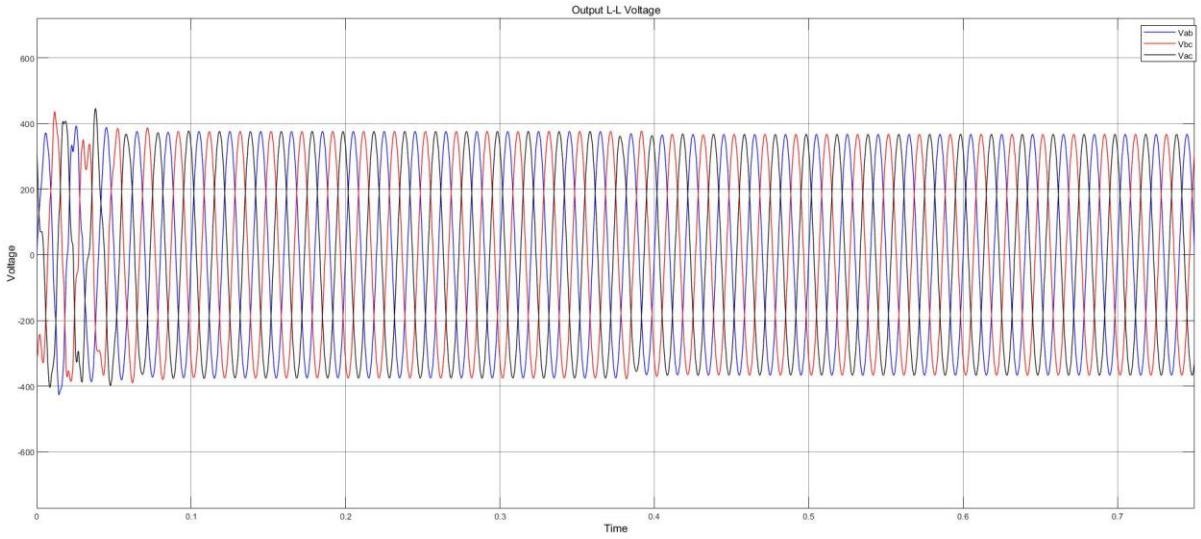


*Fig. 7-20 Output Voltage of the Inverter*

It is clear that the output voltages and currents of the inverter have the immunity against the variations of the environmental factors on the PV arrays. That is one of the most important advantages that would be considered for the HMLIs in the PV applications. Basically, there are three suggested loops that control the output voltage and current of the HMLI. The first one is the controller of the boost converter that regulates the DC-link of the inverter, the second one is the P-Q controller that controls the injected current and voltages to the grid, and the third one is the outer DC-link controller that links the output P-Q with the DC-link voltage. However, in the worst case, which is the irradiation absence (Night Mode of the inverter), the voltages and the currents of the inverter still exist, but do not have a good value of the THD.

Fig. 7-21 shows the output current perpendicular components $I_d$ and $I$. As same the output AC current, they are not affected by the changing environmental conditions, except at night mode, they have a considerable noise.

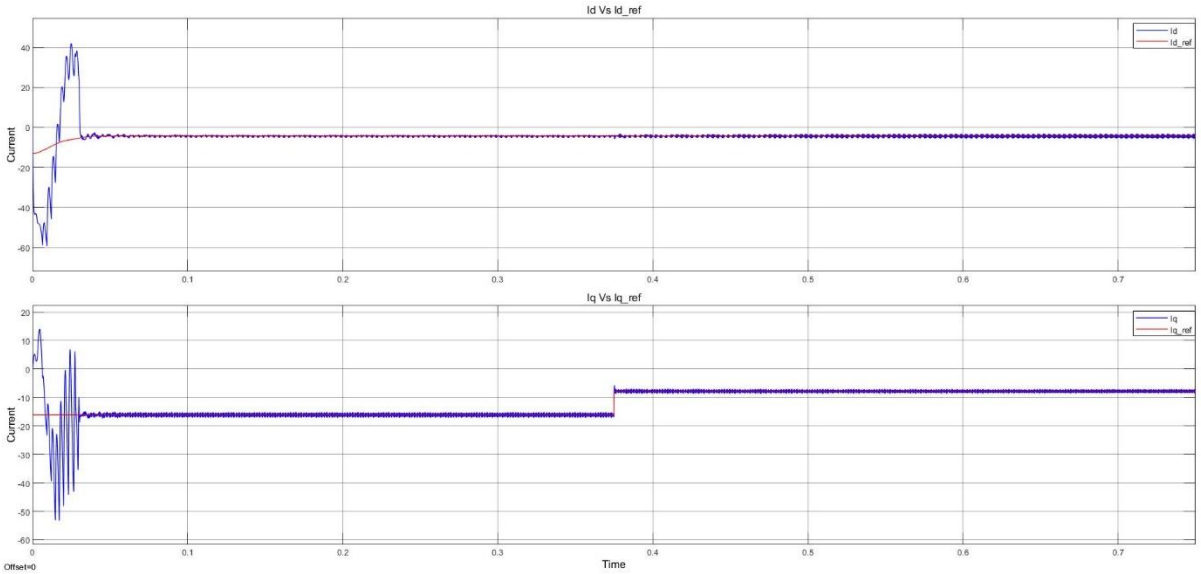


*Fig. 7-21 Id and Iq Components*

Also, Figs. 7-22 and 7-23 show the THD for the inverter output current before and after the filter.

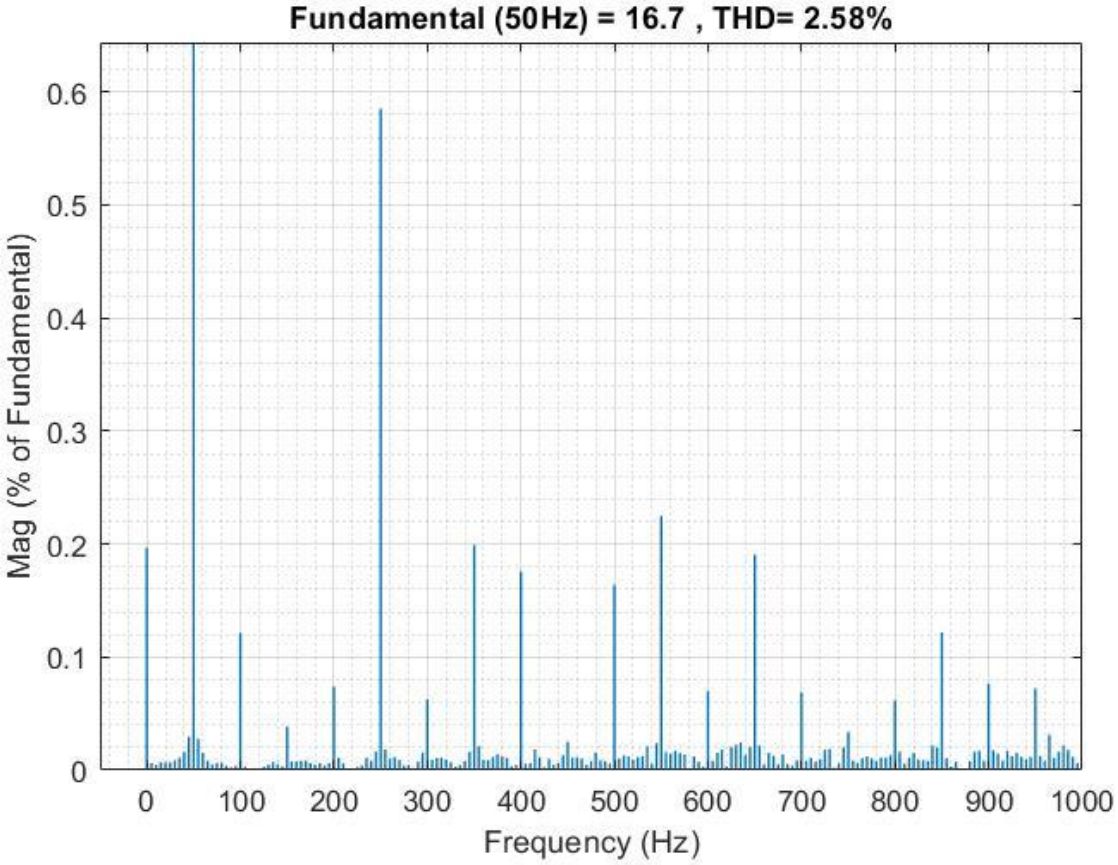


*Fig. 7-22 THD of the Output Current before the Filter*

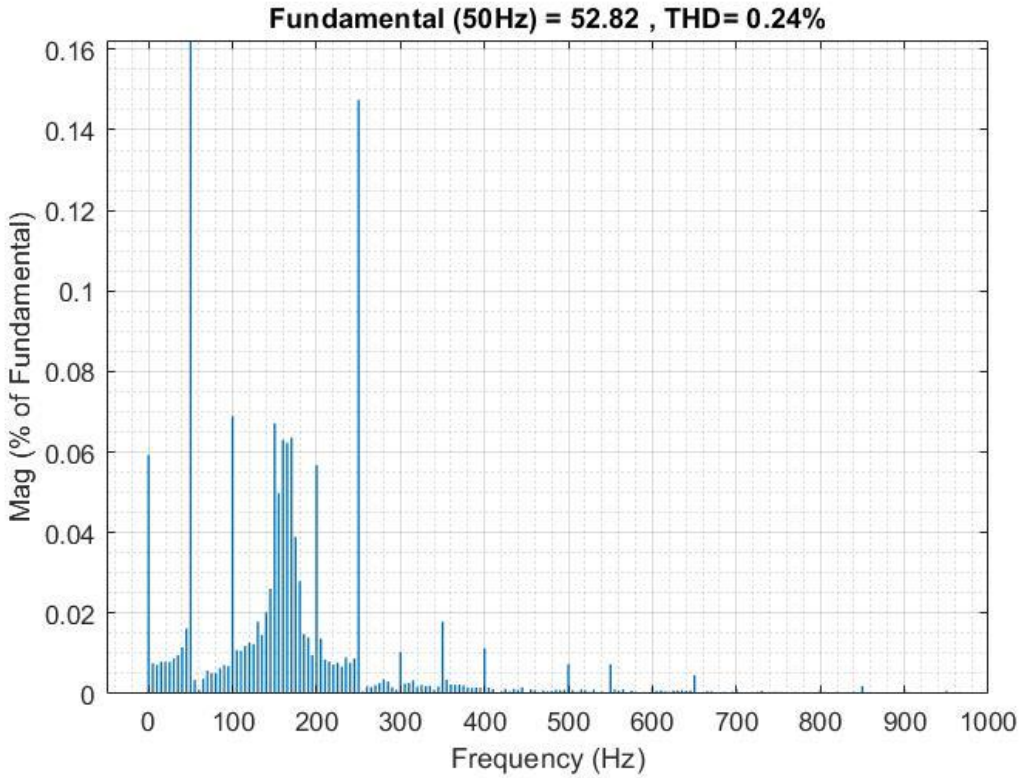


*Fig. 7-23 THD of the Output Current after the Filter*

The THD value of the output current before the filter is relatively low. The THD in the grid connected inverters must be lower than 5% [73],. But it is a very low value for the current after the filter. That proves the high efficiency of the used LCL-filter. On the other side, it is noticed that the low temperature values have a considerable effect on improving the THD value. Fig. 7-24 shows the THD spectrum of the output current. The value of the THD at 15° is 2.93%.

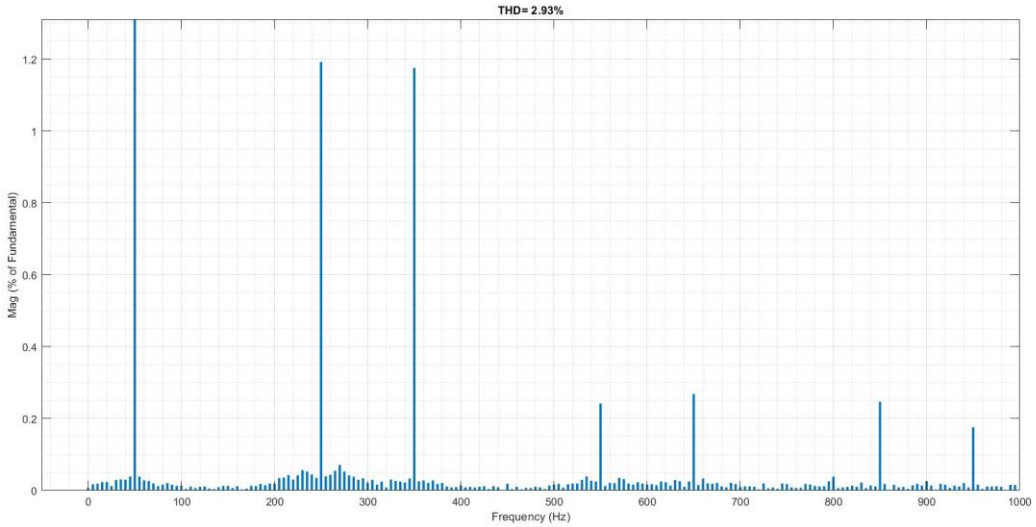


*Fig. 7-24 THD of the Output Current Before the Filter at 15 Degrees Celsius*

The output active and reactive powers corresponding to their reference values are shown in Fig. 7-25.

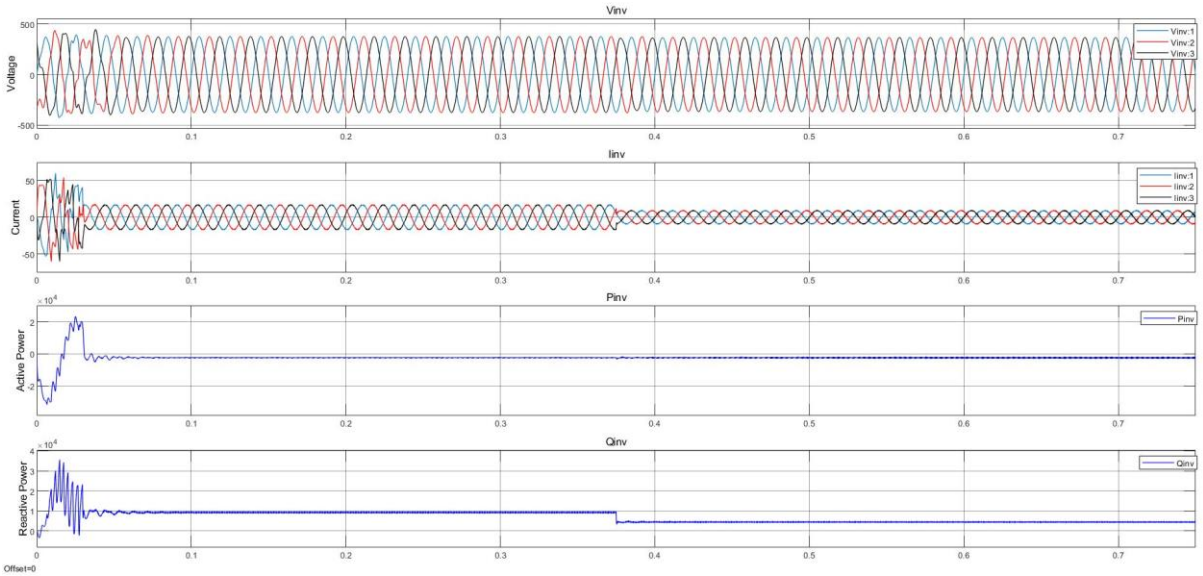


*Fig. 7-25 Output Voltage, Current, Active Power and Reactive Power*

### 7.3.2 One Phase Conditions – Simulation and Results

In this section, the effect on the inverter efficiency will be discuss only when the environmental condition is affecting one phase only (Phase A in this case.). The same irradiation and temperature value in Fig. 7-9 are applied partially to the inverter. It may be considered as a partially shading condition on phase A only. The simulation shows that there are no much differences between this case and the previous one in section 7.3.1. The considerable differences appeared only in the PV output voltages and currents as shown in Fig. 7-26.

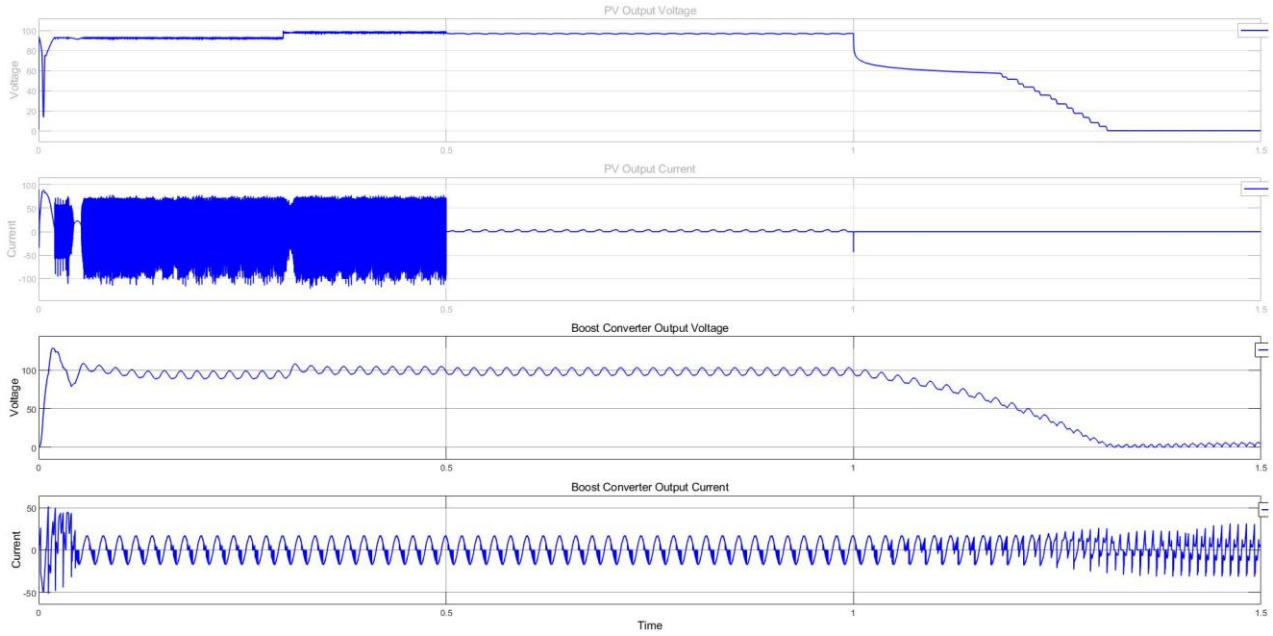


*Fig. 7-26 PV output Voltage and Current in the Partial Shading Condition*

In addition, there is a slight improvement in the THD value. Fig. 7-27 shows that the THD value decrease from 3.39% to 3.31%.

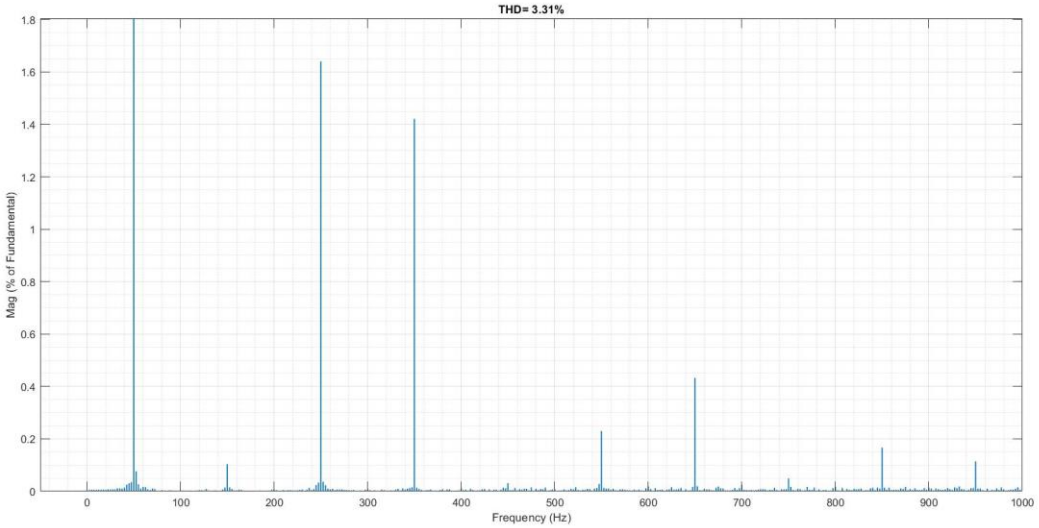


*Fig. 7-27 THD Value in the Partial Shading Conditions - One Phase*

### 7.3.3 Two Phases' Conditions – Simulation and Results

In this case, the same various environmental conditions are applied to two phases (A and B). Actually, the same results are obtained as in the one-phase case. But here, the value of the THD increases from 3.31% to 3.32% as shown in Fig. 7-28.

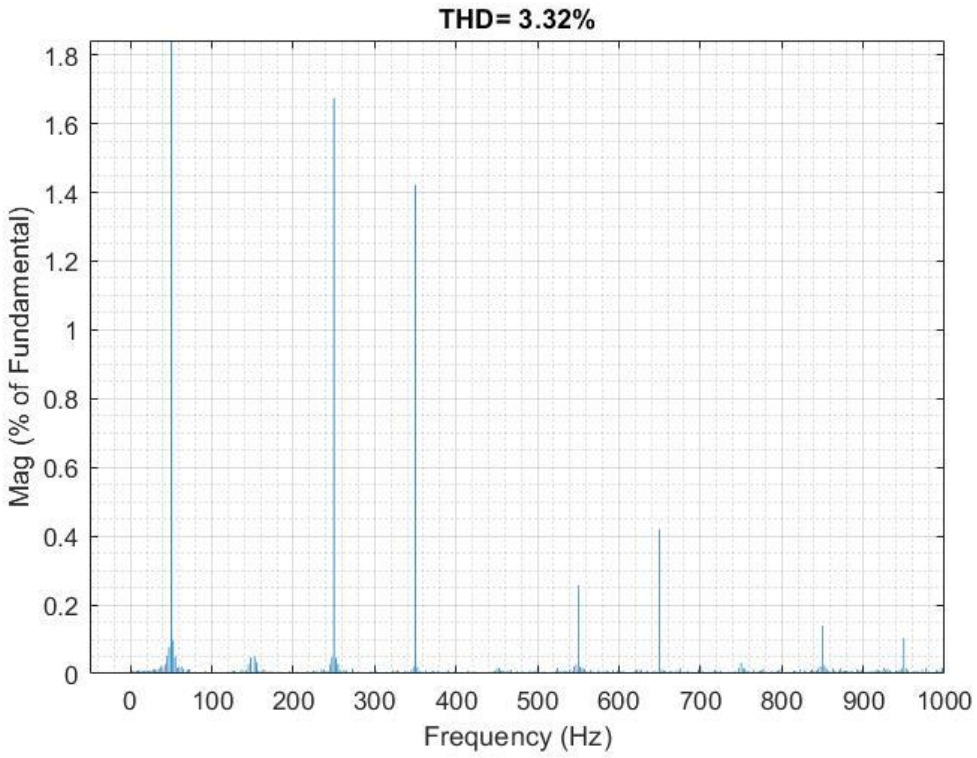


*Fig. 7-28 THD Value in the Partial Shading Conditions - Two Phases*

### 7.3.4 Output Power Injection

On the other side of the analysis, keeping the input environmental conditions at their optimal values (Irr =1000W/$m^2$ and Temp =25°) Matlab simulation results show that the grid-tied PV inverter works ideally by injecting its full power capacity to the grid. Figs. 7-29 and 7-30 show the THD values for the output current of the inverter in both cases of full and half capacities, respectively.

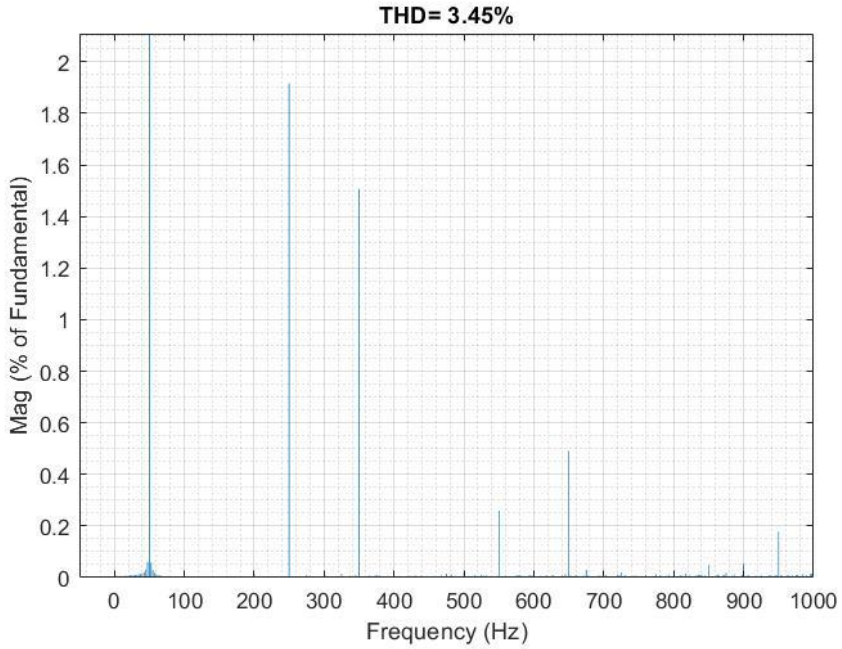


*Fig. 7-29 THD of the Output Current at the Full Power Capacity Injection*

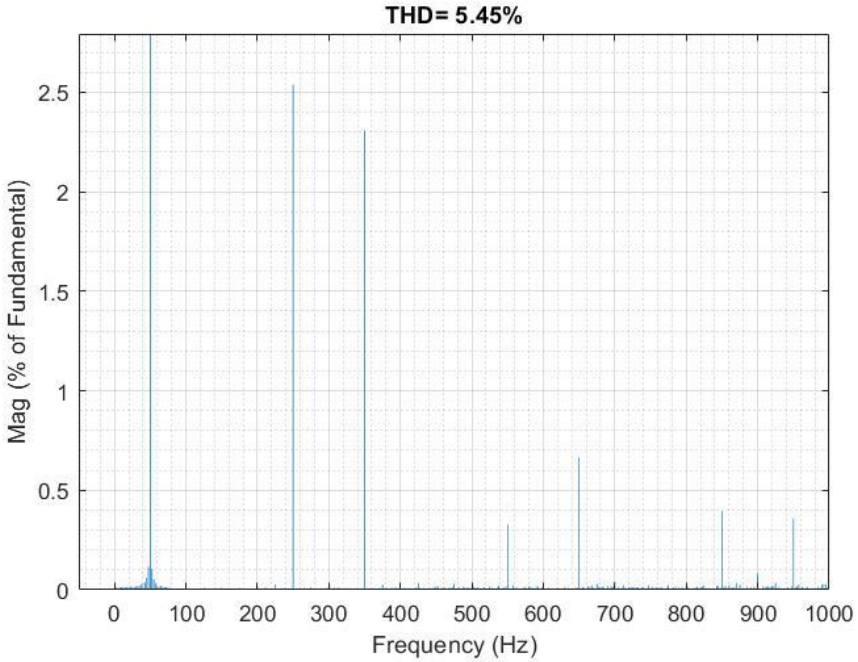


*Fig. 7-30 THD of the Output Current at the Half Power Capacity Injection*

In addition, when the power reference signal changes, the output voltage of the inverter stays constant. Whilst, the output current changes according to the power needed. That illustrates the basic concepts of the grid-tied inverters, which is to provide the same voltage as that of the grid. The output voltage of the inverter must be sinusoidal and must have the same amplitude and frequency. But the inverter current changes following the required power to be injected into the grid.

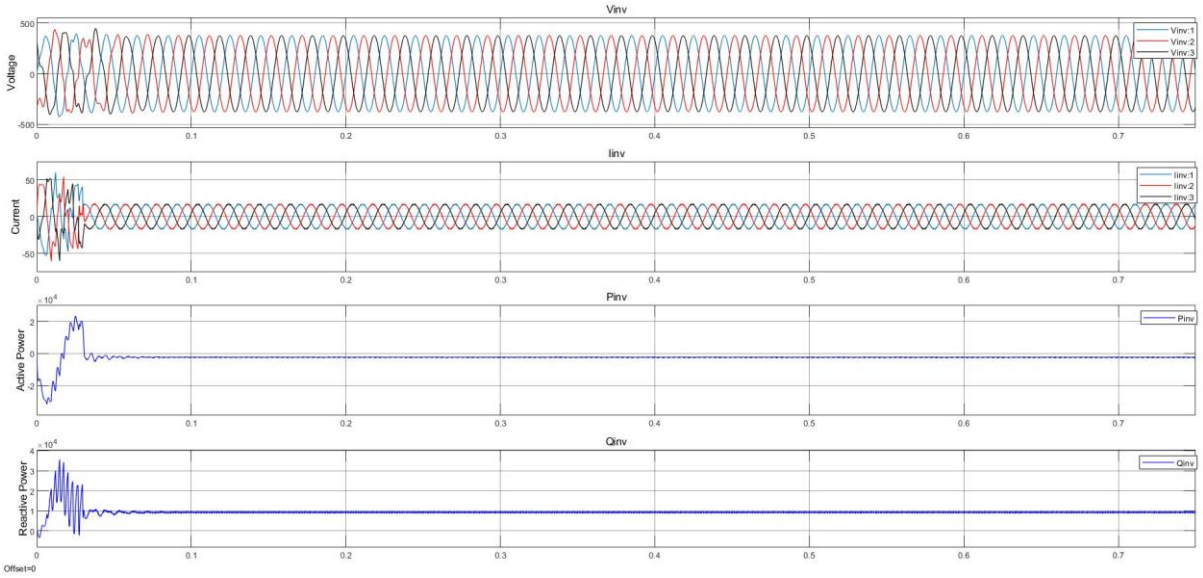


*Fig. 7-31 Power reference Effect on the Output Voltage, Current and Power*

### 7.3.5 Comparison between MLI and HMLI Inverters

Comparing the results between the Symmetrical and Asymmetrical HMLI, the results show that the THD for the HMLI is much better than the MLI under the same conditions. Fig. 7-32 shows the THD for the MLI. The value of the THD of the output current for the MLI equals 4.38%.

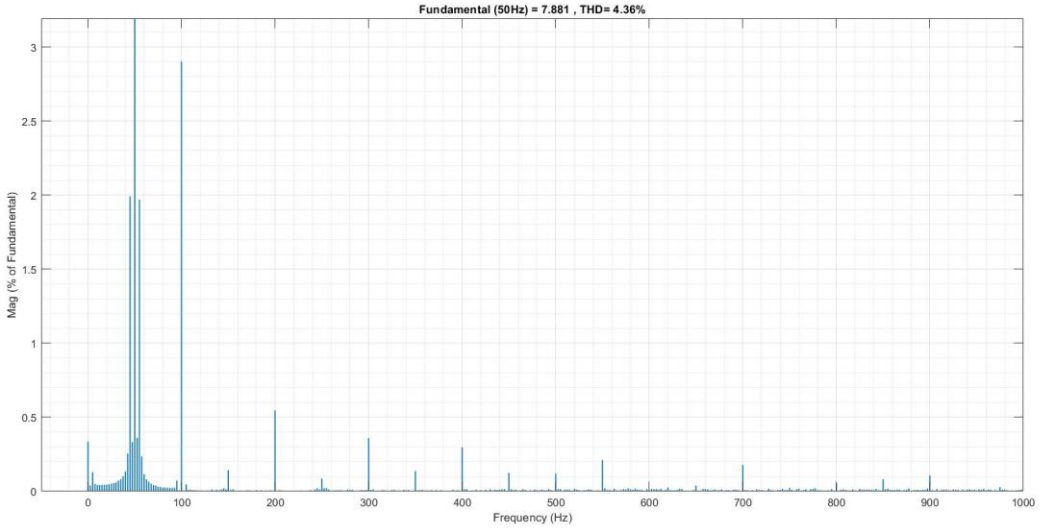


*Fig. 7-32 THD of the MLI under the same condition of the HMLI*

### 7.3.6 Grid Disconnection

Although it is naturally done, the inverter should not deliver power to the grid in case of the power outage. This case is necessary while doing maintenance works to protects engineers and technicians working directly to live parts of the grid. The inverter doesn't deliver power to the grid in the islanding case since the P-Q controller depends on the quadrant components of the grid voltage $V_{gd}$ and $V_{gq}$ and the frequency ($\omega t$). However, to deliver the power directly to the load; an off-grid controller is required. Fig. 7-33 shows that the inverter stops injecting power to the grid at the time 1 second since a breaker is opened between the inverter and the grid.

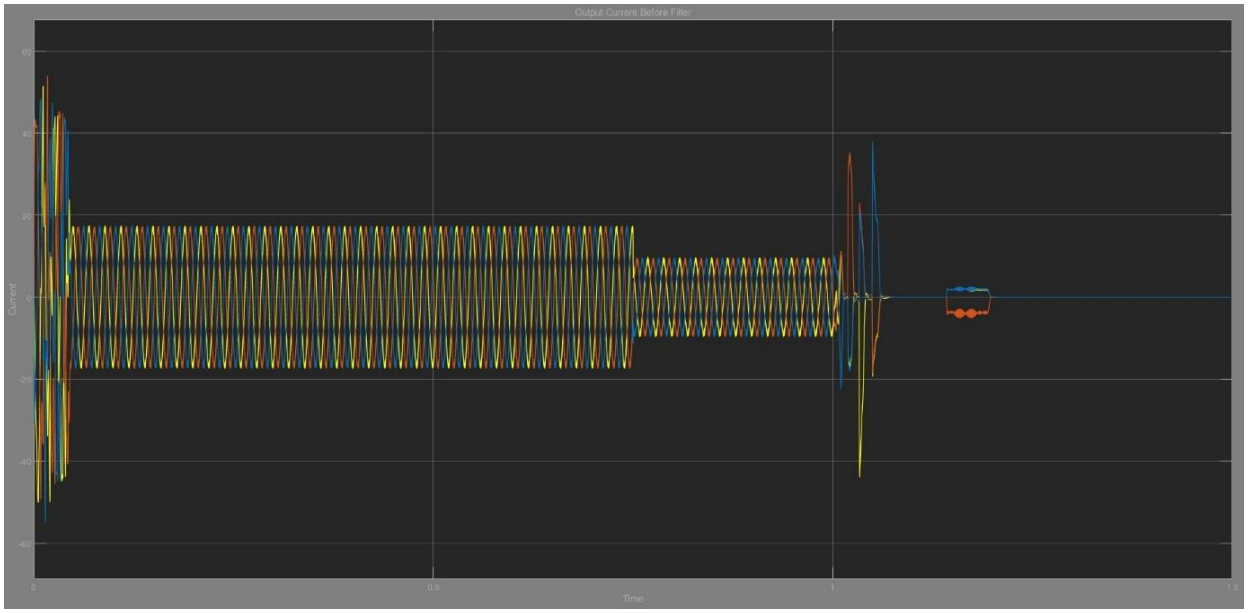


*Fig. 7-33 Grid Disconnection Case in the THMLI*

# Chapter 8. Conclusions and Future Work

## 8.1 Conclusions

In general, Hybrid Multi-Level Inverters solves most of traditional inverters drawbacks, such as the control complexity and the voltage balancing problems. They can reduce the number of the used switches; modulation techniques can be modified according to the nature of the output voltage/current. They can combine two or more traditional Multi-Level Inverter topologies and get their common advantages and produce much more levels in the output voltage/current.

Hybrid Multi-Level Inverter can be easily implemented in the PV applications. Keeping their best advantages of modularity and the same number of switching devices. However, the different-value isolated DC power supplies can be simply generated from a proper design of the PV arrays. The high number of levels in the output of the HMLI, reduces the stress across the switches, and reduces the harmonic components in the voltage waveforms.

## 8.2 Future Work

This thesis studied the HMLI in details, more and more HMLI including both voltage and Current Source Inverters may be studied. Additional focus may be paid to HMLI Current Source Inverters. Also, a detailed comparative study between all types of HMLI mentioned in the literature can be carried out, to determine which is the most appropriate type to be used in photovoltaic applications. In addition, the simulation results may be verified experimentally. On the other side, the study may be enlarged to include the study of the off-grid inverter and its controllers.

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